Projects for Veek-MT2 board in Intel Quartus Lite V20.1

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1. About names and filenames

Beware, Quartus is a Unix program that runs in Cygwin, an extensive collection of GNU and Open Source tools that provide functionality similar to a Linux distribution on Windows. Thus, all folders and files should satisfy strict Unix name rules.

The filenames can contain upper and lower case ASCII letters, numbers, dots "." and underscore "_". Do not use spaces and special characters. For completeness, some Linux versions allow them, but we have bad experiences with their usage in Cygwin. You can try to see if they work for you, but if not, complain to yourself.

We recommend using only ASCII letters and numbers in Quartus entity names. They usually correspond with filenames because one entity is stored in the file of the same filename. Its identifier must start with a letter, the last character cannot be an underscore, and two connected underscores are not allowed. However, the entity names with underscores can sometimes collapse the internal Quartus simulator run if we try it. We do not find out why. It just sometimes happens.

VHDL is not case-sensitive, but we should keep capitalization. If we define the symbol Data, the wrong style is referring to it as "data" or "DATA".

VHDL does not understand diacritics and non-ASCII characters, not even in comments.

2. Initial Configuration

Before creating the first project, you should perform permanent global configurations that will be reflected in all the following projects.

Select **Option** from Quartus menu Tools:



We start in the General tab, where we specify the default directory in which we plan to store our projects. Its choice is ours.

We recommend also checking:

"Show full file path in window titles" to improve orientation.



Then, we proceed to EDA Tool Options and set the path to ModelSim-Altera to ensure it will always be located.

We find it in subfolder

modelsim_ase\win32aloem

of the install directory. The default is:

C:\intelFPGA_lite\20.1\

🕥 Options

Category:			
✓ General	EDA Tool Options		
EDA Tool Options	Specify the directe	ory that contains the tool executable for each third-party EDA t	tool:
Fonts Headers & Ecoters Settir	EDA Tool	Directory Containing Tool Executable	
 Internet Connectivity 	Precision Synth		
Notifications	Synplify		
Libraries	Synplify Pro		
 IP Settings ID Catalog Search Loc 	Active-HDL		
Design Templates	Riviera-PRO		
License Setup	ModelSim		
Preferred Text Editor	QuestaSim		
Processing Tooltip Settings	ModelSim-Altera	C:\intelFPGA_lite\20.1\modelsim_ase\win32aloem	

×

Note: EDA abbreviation stands here for Electronic Design Automation tools that chip designers use to analyze entire semiconductor chips. The Quartus installation contains only one free tool, ModelSim Altera, i.e., ModelSim with embedded Quartus FPGA libraries.

We can also set our default browser.	Category:					
Quartus uses it to display its helps.	 General EDA Tool Options Fonts Headers & Footers Settir Internet Connectivity 	Internet Connectivity Web browser Use custom web browser instead of system default Path: "C:\Program Files\Google\Chrome\Application\chrome.exe"				
In IP Setting category, select VHDL. Note: IP is Intelligent Property here.	 IP Settings IP Catalog Search Loca Design Templates 	IP generation HDL preference: VHDL •				

If you wish, you can adjust the primary and message fonts and, eventually, other options.

OK Cancel Help

Finally, close the Option dialog by [OK] button to store changes; otherwise, they will be canceled.

Then, close Quartus Prime and rerun it so Quartus starts with new options.

3. Project Wizard of the First Project

Creating our first project is complicated by many settings, but it is one one-time task; the following projects are made in a minute; see Chapter 4 on page 12.

From the main menu Quartus, we choose File-> New Project Wizard.

🕥 Quartus Prime Lite Edition								
File	Edit	View	Project	Assignments	Proces			
	lew		Ctrl+N					
🗖 🖸	🗖 Open			Ctrl+O				
C	lose		Ctrl+F4					
A N	lew Pr	oject W	/izard					

The Wizard's dialog consists of several pages; you can scroll from one page to another, forward by [Next], and backward by [Back].

► Introduction — continue by [Next >]

► Directory, Name, Top-Level Entity

Enter any folder name inside an existing directory, e.g., "MyFirst" — the folder should not exist yet; it will be created. We also choose names for our project and entity, e.g., "Test". Do not use anything that could accidentally be an HDL language keyword, such as "else", "input", "output", and so on.

🕥 New Project Wizard	×
Directory, Name, Top-Level Entity	
What is the <u>w</u> orking directory for this project?	
C:\SPS\MyFirst	
What is the name of this <u>p</u> roject?	
Test	
What is the name of the <u>t</u> op-level design entity for this project? This name is case sensitive exactly match the entity name in the design file.	and must
Test	
Use Existing Project Settings	

After entering all items, click the [Next >] button and confirm the creation of a new directory. If you see this question, it is a good sign; Quartus projects cannot share directories.



Note 1: Quartus does not allow the storage of two projects in one folder! Each project has its directory.

Note 2: Unlike older Quartus versions, the button [Use Existing Project Settings] does not allow copying many settings in Quartus 20.1. We show the better way on page 12.

Project Types —We select Empty and press [Next >] because project templates do not exist for our educational board Veek-MT2.

Project Type
Select the type of project to create.
• Empty project
Create new project by specifying project files and libraries, tool settings.
○ Project template

► Add Files - skip by [Next >]

Family Device & Board Settings —enter the following for development board Veek-MT2:

- First, we must set the family: Cyclone IV E
- Then, we write/copy in the name filter: **EP4CE115F29C7**

In the list of available devices, we select FPGA EP4CE115F29C7 by mouse double click.

S New Project Wizard	×								
Family, Device & Board Settings									
Device Board									
Select the family and device you want to target for compilation. You can install additional device support with the Install Devices command on the Tools menu.									
To determine the version of the Quartus Prime software in which your to	arget device is supported, refer to the <u>Device Support List</u> webpage.								
Eamily: Cyclone IV E	Package: Any •								
Device: All	Pin count: Any *								
Target device	Core speed grade: Any								
○ <u>A</u> uto device selected by the Fitter	Name filter: EP4CE115F29C7								
Specific device selected in 'Available devices' list Other: n/a	☑ S <u>h</u> ow advanced devices								
A <u>v</u> ailable devices: Name Core Voltage LEs Total I/Os Gf	21Os Memory Bits Embedded multiplier 9-bit elements								
EP4CE115F29C7 1.2V 114480 529 529	3981312 532								
K	>								
	< <u>B</u> ack <u>N</u> ext > Einish Cancel <u>H</u> elp								

Click [Next>]

EDA Tools Settings – Set Model-Sim-Altera in VHDL and leave the other items in default states.

EDA Tool Se	ettings							
Specify the other EDA tools used with the Quartus Prime software to develop your project.								
<u>E</u> DA tools:								
Tool Type	Tool Name	Format(s)	Run Tool Automatically					
Design Entry/	<none> 🔻</none>	<none> -</none>	🗆 Run this tool automatically					
Simulation	ModelSim-Altera 🔹	VHDL -	□ Run gate-level simulation a					
Board-Level	Timing	<none> •</none>						
	Complete L							
	Symbol	<none></none>						
	Signal Integrity	<none> <none></none></none>						
	Signal Integrity Boundary Scan	<none> <none> <none></none></none></none>						

Click [Next >]

Summary – check if everything is OK.

🕥 New Project Wizard	×
Summary	
When you click Finish, the project will be create	d with the following settings:
Project directory:	C:\SPS\MyFirst
Project name:	Test
Top-level design entity:	Test
Number of files added:	0
Number of user libraries added:	0
Device assignments:	
Design template:	n/a
Family name:	Cyclone IV E
Device:	EP4CE115F29C7
Board:	n/a
EDA tools:	
Design entry/synthesis:	<none> (<none>)</none></none>
Simulation:	ModelSim-Altera (VHDL)
Timing analysis:	0
Operating conditions:	
VCCINT voltage:	1.2V
Junction temperature range:	0-85 °C
	< <u>Back</u> <u>N</u> ext > <u>Finish</u> Cancel <u>H</u> elp

If it is OK, click [Finish]

Additional Project Setting for Board Veek-MT2 3.1

Open the Device dialog from the Quartus menu Assignments->Device:

<

F

🕞 Qu	iartus Prime Lite Editio	n - C:/SPS/MyF	irst/Test	- Test						
File	Edit View Pr	roject Assi	ignmei	nts Pro	cessi	ng	Tools	Wir	ndow	Help
		- n 🐓	Device	2						
		/	Settin	gs				C	trl+Sh	ift+E
roje	ct Navigator A H		Assign	ment Ec	litor			C	trl+Sh	ift+A
	🕥 Device									
	Device Board									
	You can install addi To determine the v Device family Family: Cyclone IV Device: All Target device O Auto device sel	tional device suppr ersion of the Quart / E ected by the Fitter	ort with the	e Install Device	ch your ta	and on t arget de Show in Packag Pin cou Core sp Name f	the Tools m evice is sup n 'Available e: unt: peed grade ilter:	enu. ported device Any Any : Any	, refer to	
	Specific device	it View Project Assignments Processing Tools Window Help								
	O Other: n/a					Device a	and Pin Opt	tions		
	Available devices:	Com Malta an	15.	Tetelulo		10-		D ¹ 4-	F ach a	
	EP4CE115E23C8L	1.0V	114480	281	281	ius	3981312	DITS	532	
	EP4CE115F23C9L	1.0V	114480	281	281	1	3981312		532	
	EP4CE115F23I7	1.2V	114480	281	281	1	3981312		532	
	EP4CE115F23I8L	1.0V	114480	281	281	1	3981312		532	
	EP4CE115F29C7	1.2V	114480	529	529	3	3981312		532	

We saw this dialog in Project Wizard, but now, the new button [Device and Pin Options] appears here. Click on it and select in the Dual-Purpose Pins tab that nCEO pin of FPGA will be used as regular I/O.

General	Dual-Purpose Pins					
Configuration Programming Files Unused Pins	Specify how dual-purpose settings for each pin depe which is: Active Serial	pecify how dual-purpose pins should be used after device configuration is complete. The default ettings for each pin depend on the current configuration scheme selected in the Configuration tab, /hich is: Active Serial				
Dual-Purpose Pins	Dual-purpose pins:					
Capacitive Loading Board Trace Model	Name	Value				
I/O Timing	DCLK	Use as programming pin				
Voltage	Data[0] As input tri-stated					
Pin Placement	Data[1]/ASDO	Data[1]/ASDO As input tri-stated Data[72] Use as regular I/O FLASH_nCE/nCSO As input tri-stated Other Active Parallel pins Use as regular I/O				
Error Detection CRC	Data[72]					
CvP Settings	FLASH_nCE/nCSO					
Partial Reconfiguration	Other Active Parallel pins					
	nCEO	Use as programming pin				
		Use as programming pin				
		Use as regular I/O				
		-				
		. ↓				
		-				

By [OK] buttons, we first close the sub dialog "Device and Pin Options" and then the "Device" dialog.

Note: Pin nCEO (Chip Enable Output) serves in JTAG communication as the selection of an FPGA device, to which we download configuration. VEEK-MT2 board contains only one FPGA chip, which is always selected. Its printed board utilizes nCEO as an LCD input; therefore, we must inform Quartus about this modification.

3.2 TimeQuest Setting

Download zip-file from our web site:

https://dcenet.fel.cvut.cz/edu/fpga/veek-mt2/VEEKMT2_Assignments.zip

and unpack it into the directory of the created project.



Invoke the Settings dialog from the Quartus menu:

S Quartus Prime Lite Edition - C:/SPS/MyFirst/Test - Test									
File	Edit	View	Project	As	signments	Processing	Tools	Window	Help
			-/- n	•	Device				
÷ 🛄			0	2	Settings			Ctrl+Sh	ift+E
Projec	t Nav	igator <mark>/</mark>	Hierarch	4	Assignme	nt Editor		Ctrl+Sh	ift+A
		Er	ntity:Instar	4	Pin Planne	er		Ctrl+Sh	ift+N
A Cy	clone	IV E: EF	4CE115F		Remove A	ssignments			
-	lest			1	Back-Anno	otate Assignm	nents		

In the tree Category of the dialog Settings, select EDA Tool Settings. Set up the simulation tool to ModelSim Altera in VHDL. Do not change anything else here! The free version does not contain other EDA programs.

🚽 Settings - Test								
Category:								
General	EDA Tool Settin	gs						
Files	Specify the other EDA tools used with the Quartus Prime software to develop your							
Libraries								
✓ IP Settings	EDA tools:							
IP Catalog Search Locatic	Tool Type	Tool Name	Format(s)	Run Tool Automa				
Design Templates	Design Entry/	<none> •</none>	<none></none>	🗆 Run this tool au				
 Operating Settings and Cor 	Simulation	ModelSim-Altera 🔻	VHDL -	🗆 Run gate-level :				
Voltage	Board-Level	Timing	<none> -</none>					
Temperature	board Ecver			1				
 Compilation Process Setting 		Symbol	<none> •</none>					
Incremental Compilation		Signal Integrity	<none> -</none>					
✓ EDA Tool Settings		Boundary Scan	<none> •</none>	1				
Design Entry/Synthesis		boundary ocur						

In the category Compiler setting -> VHDL input, check VHDL 2008.



In Timing Analyzer category, we browse for files *.sdc (Synopsys Design Constraints) that were previously extracted from the zip archive.

Settings - Test						—	
Category:						De	evice/B
General	Timing Anal	yzer					
Files	Specify Tim	ing Analyzer opti	ions.				
Libraries	606 ft 1						
✓ IP Settings	-SDC files to	o include in the p	project				
IP Catalog Search Locatic	File name						Add
Design Templates	The nume	•					Auu
 Operating Settings and Cor 	•	Select File					
Voltage	File Nam		242 »	> MyFirst	- ēi	O Search MyFirst	
Temperature				, myrnae	÷ U	- Scaren Myrinsk	
 Compilation Process Settin_{ 		Organize 🔹 Ne	ew folder			==	•
Incremental Compilation		1.0.11	^	Name	^	Date modified	1
✓ EDA Tool Settings		Quick access		db		11.10.2023 15:24	F
Design Entry/Synthesis		lene One Drive		VeekMT2.sdc		11.10.2023 16:08	5
Simulation		💻 This PC		VeekMT2_LCD.sdc		11.10.2023 16:08	5
Board-Level	🗹 Enable Ad	3D Objects					
✓ Compiler Settings	-Tcl Script	📃 Desktop					
VHDL Input	Tal Carlet	🔮 Documents					
Verilog HDL Input	i ci Script	👆 Downloads					
Default Parameters	🗹 Run def	👌 Music					
Timing Analyzer	Matastabil	Pictures					
Assembler	Metastabit	📲 Videos					
Design Assistant	Synchroniz	SYSTEM (C:)					
Signal Tap Logic Analyzer		👝 Data (E:)	~ <	r			
Logic Analyzer Interface	Description:		File nar	ne: "VeekMT2 LCD.sdc	"VeekMT2.sdc"	Synopsys Design Co	onstraints l
Power Analyzer Settings	Associates					Open	Cance
SSN Analyzer						open	cance

We select them both. They add to the list of Timing Analyzer constraints.

Specify Timing Analyzer options.							
SDC files to include in the project							

Note: The *.sdc files tell Quartus that the educational board VEEK-MT2 contains a clock generator with a frequency of 50 MHz. The clock frequency is a critical specification. Without this information, our circuit will be compiled for a default frequency of 1 GHz. And the internal FPGA connections depend on frequency, as we explain in our lectures, so that the result will be nonfunctional.

Finally, we close the Setting dialog by the **[OK] button** to accept data.

3.3 Pin Assignments

FPGA chip used in VEEK-MT2 has 780 solder balls arranged in a grid or array at the bottom of the package body for external electrical connections; see the left picture [source Intel]. Each solder ball is internally one pin.

Users can direct inputs or outputs of their circuit designs up to 528 pins. This possibility can simplify printed board designs. The pins are indexed with a letter and a number. We can see them in Pin Planner.





We work with a ready-made board; therefore, we must follow their placement by loading the manufacturer's pin assignments. Their absence is a frequent error in beginner's designs. Always check if the Assignment Editor shows pins and not an empty list as below:

Quartus Prime Lite Edition - C:/SF	PS/MyFirst/Test - Tes	t									
File Edit View Project	Assignments	Processing	Tools	Window	Help						
	DeviceSettings			Ctrl+Sh	ift+E	×	 		🕨 🔸 🤞	tor) 📇 🄇
	🧳 Assignme	ent Editor		Ctrl+Sh	ift+A	H	< <net< td=""><td>w>> ▼</td><td>er on node na</td><td>ames: *</td><td></td></net<>	w>> ▼	er on node na	ames: *	
 Cyclone IV E: EP4CE115F Test 	 Pin Planner Remove Assignments Resk Appetete Assignments 			Ctrl+Shift+N			tatu 1	From < <new>></new>	To < <new>></new>	Assignm	ient Nan
	Back-Ann	iotate Assignn	ients								

The original pin indexes are complex to remember, so we import their association with their symbolic names defined by the Pin Assignment spreadsheet table. In the main Quartus menu, select:

Assignments->Import Assignments.

Quartus Prime Lite Edition - C:/SPS/MyFirst/Test - Test

Edit View Project Assignments Processing Tools Window Help Device... 📄 🗖 🔚 🤟 Ctrl+Shift+E Settings... Project Navigator Ctrl+Shift+A Assignment Editor Pin Planner Ctrl+Shift+N Cyclone IV E: EP4CE115F Remove Assignments... 🔹 Test 👛 Back-Annotate Assignments.. Import Assignments. Export Assignments... Assignment Groups...

In the Import Assignment dialog, we browse for the download file VeekMT2_PinAssignments.csv.

🕥 Quartus Prime Lite Edition - C:/SPS/MyFirst/Test - Test	
File Edit View Project Assignments Processing Tools Wir	ndow Help
□ □ ★ □ ★ □ ★ ★ □ ★ ★ ★ ★ ★ ★ ★ ★ ★ ★ ★ ★ ★ ★ ★ ★ ★ ★ ★	
Project Navigator Alierarchy	▼ Q 및 & ×
Entity:Instance	Select File
Cyclone IV E: EP4CE115F29C7	$\leftarrow \rightarrow \checkmark \uparrow$ \backsim « SPS » MyFirst » \checkmark \circlearrowright \checkmark Search MyFirst
Test Import Assignments	Organize ▼ New folder
Charity the source and estagories of assignments to import	3D Objects A Name Date modifie
File name:	Desktop db 11.10.2023 17 Documents Do
Copy evicting assignments into Test get bak befor	↓ Downloads ☐ Test.qsf 11.10.2023 16
Copy existing assignments into rest.qsi.bak befor Advanced	Music VeekMT2.sdc 11.10.2023 16
OK Cancel Help	Pictures VeekMT2_LCD.sdc 11.10.2023 16 VeekMT2 DinArrignments cs/ 11.10.2023 16
	Videos
	SYSTEM (C:) V <
	File name: VeekMT2_PinAssignments.csv V Import Files (*.qsf *
	Open

We confirm the choice by [Open] and then [OK] buttons.

We have no assignment yet, so we unchecked the copy option. We import by [OK].

S Import Assignments	×
Specify the source and categories of assignments to import.	
File name: C:/SPS/MyFirst/VeekMT2_PinAssignments.csv	Categories
Copy existing assignments into Test.qsf.bak before importing	Advanced
OK Cancel	l Help

If we look at **Assignments-> Assignment Editor**, the list now contains associations. We can find out that PIN_G18 from the previous pin planner figure was named HEX0[0], i.e., it is the upper led segment in the least significant 7-segment digit :-)

🕥 Quartus Prime Lite Edition - C:/SPS/MyFirst/Test - Test							_	
File Edit View Project Assignments Pro	cessin	g To	ools Windo	w Help			Search altera.c	om 📀
<u> こ に 日 ゲ D 前 っ に</u>	Test			• 🗹 🎸	🥳 ⊗ 🔊 🕨	🖌 🛧 🇳) 🚫 🚠	» 🤿
Project Navigator 🍌 Hierarchy 🔹 🤉 🖓 🗗 🗙	4		Assign	ment Editor	×			
Entity:Instance	< <n< td=""><td>ew>></td><td>• ▼ 🗹 Filter</td><td>on node name:</td><td>s: *</td><td>~ Cate</td><td>egory: Locatio</td><td>ons 🔻</td></n<>	ew>>	• ▼ 🗹 Filter	on node name:	s: *	~ Cate	egory: Locatio	ons 🔻
A Cyclone IV E: EP4CE115F29C7		tatu	From	То	Assignment Name	Value	Enabled	Enti ^
Test ^h	343	 Image: A second s		🔷 LEDR[15]	Location	PIN_G15	Yes	
	344	 Image: A second s		🔷 LEDR[16]	Location	PIN_G16	Yes	
	345	 Image: A second s		🔷 LEDR[9]	Location	PIN_G17	Yes	
	346	<		HEX0[0]	Location	PIN_G18	Yes	
	347	<		LEDR[0]	Location	PIN_G19	Yes	~
	<							>
Image: Second state Image: Second state				🍀 Find 👪	Find Next			
 Type ID Message 21648 Please refer to Package Ou 140120 Import completed. 1202 as 	tline signme	Draw ents (ing (POD) fo were written	or any mechani n (out of 1202	cal enablement at http read). O non-global	os://www.inte assignments	l.com/content, were skipped b	/www/us/en because of

It was the last setting. We have our first project.

~ 0 ~

Never edit the pin assignment list; keep compatibility by using predefined names!

4. The Express Copy of a Created Project

If I have already created at least one complete project from scratch, we can copy it to obtain another project in a minute.

From the Quartus menu, we open any of our projects, e.g., we use MyFirst:

🕞 Quartus Prime Lite Edition		🕥 Quartus Prime Lite Edition	
File Edit View Project	Assignments Proce	S File Edit View Project Assignments Processing Tools Window He	elp
New	Ctrl+N		
🔁 Open	Ctrl+O	Organize New folder	Search Myr
Close	Ctrl+F4	Program Files (Name Date modified	Туре
\Lambda New Project Wizard		Pub_inc db 13.10.2023 14:45 Qt Qt output_files 13.10.2023 14:34	File folc File folc
😤 Open Project	Ctrl+J	> sigasi ♥ Test.qpf 10.10.2023 12:57	QPF File
		File name: Test.qpf	artus Prime Pi
			Open

Eventually, we can access it from the "Recent Project" offer:

0	Quartus Prime Lite E	dition						
File	e Edit View	Project	Assignments	Proce	ssing	Tools	Window	Help
	New		Ctrl+N					- /
~	Open		Ctrl+O			_	_	
	Close		Ctrl+F4					
A	New Project W	/izard						
×	Open Project		Ctrl+J					
	Save Project							
	Close Proiect				-		-	
	Recent Files			· ·				
	Recent Project	ts		•	1	C:/SPS/	MyFirst/T	est.gpf

First, we select "Project-> Clean project" to remove all temporary files, and by [OK], we confirm either the default option or All revisions.

🕥 Quartus Prime Lite E	dition - C:/SPS/MyFirst/Test - Test	🕥 Clean Project 🛛 🗙
File Edit View	Project Assignments Processing Add Current File to Project	O All revisions Revision name: All revisions removes the project database and other files generated
Er Cyclone IV E: EF Test	Copy Project Clean Project	by the Quartus Prime software, including report and programming files.

Then, we open the "Project->Copy Project" dialog. We enter our project name, e.g., Test2, and specify a directory where we want to store its files.

🕥 Quartus Prime Lite Edition - C:/SPS/MyFirst/Test - Test			🕥 Quartus Prime Lite Edition - C:/SPS/MyFirst/Test - Test					
File Edit View	Project	Assignments Process	File Edit View Project Assignments Processing Tools Window He					
	Add C	Current File to Project Remove Files in Project	Copy Project					
Project Navigator	🗗 Revisi	ions	New project name: Test2					
En	Сору	Project	☑ Open new project. (This option closes the current project.)					
 Cyclone IV E: EP Test ⁴ 	Clean	Project	Cyclone IV E Test Cancel He					

After confirming our choice by [OK], the message below signals that we are creating our project in the new directory, which will be its own, as required.

🕥 Quartus Prim	ne Lite E	dition - C:/SP	S/MyFirst/Test - Te	st			
File Edit	View	Project	Assignments	Processing	Tools	Window	Help
🗖	. `	Copy Projec	t				×
Proiect Navig	D	estination	directory: C:	/SPS/MyNext/	1		
	N	ew projec	t name: Te	est2			
À Cyclone I\	Q	uartus Prime					×
✤ Test [♣]	<u> </u>	Destina you wa	ation director Int to create it	y "C:/SPS/MyN ?	lext/" do	oes not exi	st. Do
					Y	′es	No

We have already created our new project with all the necessary settings. It also contains all the Test project files.

The following chapter explains how

- to change Top-Level Entity;
- to adjust our project by adding new files or removing unused ones;
- to move our project to another directory or computer;
- to change the compilation result file name.

5. Working with Projects

The following steps are more adjustments than requirements.

5.1 Reorganizing files in Project Navigator

From the file dialog, we can reorganize files in our project.

🕥 Quartus Prime Lite Edition - C:/SPS/MyNext/Test2 - Test2										
File Edit	t View	Project	Assignments	Processing	Tools	Window	He			
		Ade	d Current File to	Project						
		😤 Ado	d/Remove Files i	n Project						
Project Na	vigator	🗗 Rev	visions				1			
	имт <u>р</u> I (Cop	oy Project							
	kMT2_L	Cle	an Project							

It is possible to add new files or remove ones no longer needed. The changes are performed only in the list. Files are not deleted from the hard drive; any file explorer can do it.

We always keep all our design files in the directory of the project. We easily recognize wrongly placed items by their extra path.

In the left figure, wrongly located files are marked by red box. The first one

../MyFirst/DisplayOff.vhd

is in the parent's subfolder:

C:/SPS/MyFirst/DisplayOff.vhd

i.e., outside our project.

The second file

E:/@QUARTUS/Font_Rom.vhd

is stored even on a different drive.

The third file

counter.vhd

is in a subfolder output_files of our project. It is acceptable but not recommended for small projects.

The preferable file locations are in the project directory, i.e., without paths.





Eventually, we can rearrange the Project Navigator list with buttons [Up] or [Down]. Then, we confirm the changes by clicking [OK] button.



5.2 How to specify Top-Level Entity

Our Top-Level Entity selects the design file from which the compilation begins. After we write down some synthesis files, we can dedicate anyone as the Top-Level Entity from the Project Navigator Files.

For instance, we add DisplayOff.vhd, extracted from the zip mentioned in Chapter 3.2 on page 8, and create a simple **Demo.bdf** that copies slider switches to red LEDs. Then, we mark it as a Top-Level entity from its context menu (a right mouse click on file).



5.3 Moving and zipping our project

Quartus is very versatile. We can open a project created in version 20.1 in some of its previous versions, e.g., in Quartus 13.1, and any lower version project in upper Quartus.

If we have all files in the project directory, as was explained in the previous chapter, Quartus keeps their path relative. So we can rename the project's root directory or move it to another location.

When we move our project to a different computer, directory, or Quartus version, we can see a message similar to the picture below:



We should always confirm [YES] if we have a small project.

Note: Compiling huge industrial designs can sometimes last for several hours. Therefore, the Quartus asks if we allow deleting previous results. It is better to let the Quartus begin with clean intermediate databases in small projects.

However, our tiny project can surprisingly contain many temporary files created during compilation and placement into an FPGA chip; see the figure below.

The project with Quartus compiler temporary files

MyNext Properties						
General Sha	rring Security Previous Versions Customize					
	MyNext					
Туре:	File folder					
Location:	C:\SPS					
Size:	7,55 MB (7 924 207 bytes)					
Size on disk:	n disk: 7,71 MB (8 085 504 bytes)					
Contains:	117 Files, 6 Folders					

without the Quartus compiler temporary file

MyNext Properties								
General	Sharing	Security Previous Versions Customize						
MyNext								
Type:	Type: File folder							
Location	n: C:	C:\SPS						
Size: 202 KB (207 760 bytes)								
Size on	disk: 24	244 KB (249 856 bytes)						
Contain	s: 31	Files, 4 Fo	olders					

Even if our design had a few files, the FPGA is big. The compiler needs to configure everything in its whole chip, i.e., in our case, it mostly deactivates non-used parts.

We can reduce the project size by removing temporary files before zipping or copying the project to a USB stick by the Project -> Clean Project, equivalent to the "make clean" command in classic programming.



Any of the selections below leads to removing all Quartus compiler temporary files.

🕥 Clean Project	×	🕥 Clean Project
○ All revisions		 All revisions
Revision name: *	~	○ Revision name: *
Note: Cleaning revisions removes the	2	Note: Cleaning revisions remove
project database and other files gene	erated	project database and other file
by the Quartus Prime software, inclu	ding	by the Quartus Prime software,
report and programming files.		report and programming files.
OK Cancel	Help	OK Cancel

Then, we close the Quartus to release its locked files and run the File Explorer.

We select the Send to->Compressed (zipped) folder from the context menu of the root directory folder.

> This PC > SYSTEM (C:) > SPS					The result of	the compress	ion:	
lame ^	Date	Туре	Size	Tags	SPS	Extract		
MyFirst	10.10.2023 12:36	File folder			Share View	Compressed Folder	Tools	
- MyNext	13.10.2023 15:35	File folder						
Open		Ider			> This PC > SYS	TEM (C:) > SPS		5 V
Open in new v	window	lder				<i>c</i> :	-	
en la presidente	NO STOLEN AND STOLEN	THE REPORT	0.000000		Name	Size	lype	
Pin to Start	,				MyNext.zip	58 KB	Compres	sed (zipped)
Send to		> Blueto	ooth device					
Cut		Comp	oressed (zipped) fo	lder				
Copy		E Deskte	op (create shortcut	t)				

Note: We prefer zip to the Quartus menu command the "Archive Project":

🕥 Quartus Prime Lite Edition - C:/SPS/MyNext/Test2 - Test2									
File Edit View	Project		Assignments	Processing	Tools				
	8	Add Add	Current File to /Remove Files i	Project n Project					
Project Navigator	ø	Revisions							
En		Copy Clea	/ Project n Project						
Demo	÷	Arch	Archive Project						
		Rest	Restore Archived Project						

Its result has an internal format *.qar that can be depacked only by Quartus. The zip file is more versatile.

5.4 Changing Revision = Compilation Result Filename

The compilation generates the result, which filename is derived from the revision name. For example, the result can be **Test.sof** (sof=SRAM Object File). The Revision is also copied with the project. We can quickly change it from the Revision dialog:

🕥 Quartus Prime Lite Edition - C:/SPS/MyNext/Test2 - Test		🕥 Revisions							
File Edit View	Project Assignments Processing Add Current File to Project				Specify the current revision for the project, create a new revision, de existing revision, or edit the description of a revision.				
Project Navigator	Remove Files in Project			Revisions:					
	🗗 Revi	sions			Revision Name	Top-level Entity	Family	Device	
Cyclone IV E: EF	Cop Clea	y Project n Project			✓ Test < <new revision="">></new>	Test	Cyclone IV E	EP4CE115F29C7	
- lest	• • •				<			>	

By mouse double click into <<new revision>> table row, we open sub dialog:

🕥 Quartus Prime Lite Edition - C:/	SPS/MyNext/Test2 - Test			
File Edit View Project	t Assignments Pro	ocessing Tools	Window Help Create Revision	×
Project Navigator A Hierar	chy र ्∎ वि अ	Specify a name and description for the new revision. You can base the		
Entity:Inst	ance 5F29C7	revision on an existing revision, and specify the revision as the current revision		
Test ⁴	S Revisions		Pavicion name: Tact2	
	Specify the curren existing revision, o	t revision for the p r edit the descript	Based on revision: Test	•
	Revisions:		Description:	_
	Revision Name	Top-level Entity	Created from MyFirst Test	
	🗸 Test	Test		
	< <new revision="">> <</new>		☑ Copy database	
			☑ Set as current revision	
			OK Cancel Help	

We enter, for example, Test2 as the name of our new project and possibly some description if we wish. After confirming by [OK], we again open the menu: Project ->Revisions.

🕥 Qua	artus Pri	me Lite Ed	lition - C:/SPS/MyNext/T	fest2 - Test2							
File	Edit	View	Project Assignm	nents Processing	Tools Win	dow Help					
			🕥 Revisions				-				
Projec	t Navi	gator 🍐	Specify the curr existing revision	Specify the current revision for the project, create a new revision, delete an existing revision, or edit the description of a revision.							
		En	Revisions:								
▲ Cyo ●	clone Test	IV E: EP	Revision Name	Top-level Entity	Family	Device	^	Set Current			
			✓ Test2	Test	Cyclone IV E	EP4CE115F29C7		Delete			
			Test	Test	Cyclone IV E	EP4CE115F29C7	J	Compare			
			<	1		>	·				

After deleting the old revision Test, we obtained the project, which compilation leads to Test2.sof.

Revisions			-	- 🗆 X					
Specify the current revision for the project, create a new revision, delete an existing revision, or edit the description of a revision.									
Revisions:									
Revision Name	Top-level Entity	Family	Device	Set Current					
✓ Test2	Test	Cyclone IV E	EP4CE115F29C7	Delete					
< <new revision<="" td=""><td></td><td></td><td></td><td>Compare</td></new>				Compare					
<			>	•					
		ОК	Cancel Appl	y Help					

The result Test2.sof can be downloaded into the FPGA chip by the Quartus programmer.

📙 🛛 🔁 📙 🖵 🕴 output_files								
File Home Share	View							
\leftarrow \rightarrow \checkmark \uparrow \bullet This PC \Rightarrow SYSTEM (C:) \Rightarrow SPS \Rightarrow MyNext \Rightarrow output_f								
✓ MyNext	▲ Name	Size						
db	Test2.sta.summa	ary 1 KB						
> 🔤 incremental_db	Test2.sta.rpt	105 KB						
output_files	😋 Test2.sof	3 459 KB						
> 📙 simulation	Test2.sld	1 KB						

The Quartus menu: Tools->Programmer shows the dialog below.

Programmer - C:/SPS/MyNext/Test2 - Test2 - [C:/SPS/MyNext/output_files/Test2.cdf]										
File Edit Viev	v Processing Tools \	Window Help			S					
Hardware Setup USB-Blaster [USB-0] Mode: JTAG										
M Start	File	Device	Checksum	Usercode	 (
[■] Stop	output_files/Test2.sof	EP4CE115F29	00565B1F	00565B1F						
🏓 Auto Detec	<									

We explain its setting in practical exercises of our LSP course. Its brief explanation is on page 40 of the document:

https://dcenet.fel.cvut.cz/edu/fpga/de2-115/My_First_Fpga.pdf

Note: VEEK-MT2 is a combo of LCD and DE2-115 board; thus, DE2-115 manuals are valid, but DE2-115 Pin Assignments define only a part of VEEK-MT2 pin assignments.

The programmer more advanced functions, which we do not use in the LSP course, are described in the Intel document:

https://www.intel.com/content/www/us/en/docs/programmable/683039/20-4/introduction.html