Projects for Veek-MT2 board in Intel Quartus Lite V20.1 or V23.1

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Czech Technical University in Prague

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1. About names and filenames

Beware, Quartus is a Unix program that runs in Cygwin, an extensive collection of GNU and Open Source tools that provide functionality similar to a Linux distribution on Windows. Thus, all folders and files should satisfy strict Unix name rules.

The filenames can contain upper and lower case ASCII letters, numbers, dots "." and underscore "_". Do not use spaces and special characters. For completeness, some Linux versions allow them, but we have bad experiences with their usage in Cygwin. You can try to see if they work for you, but if not, complain to yourself.

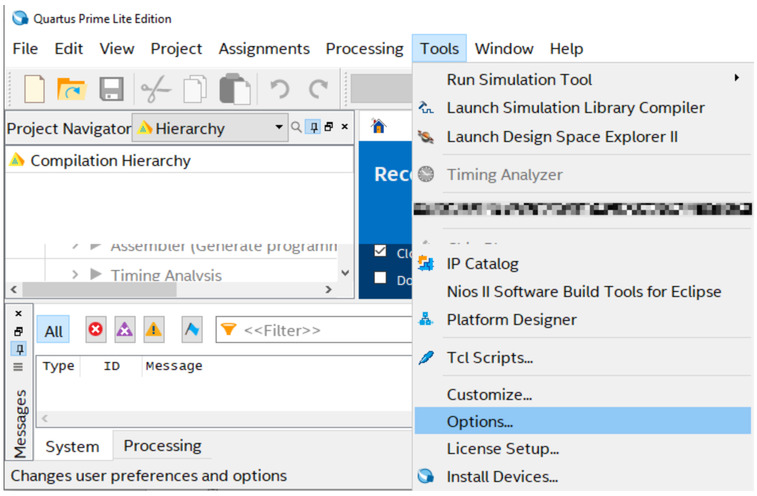
We recommend using only ASCII letters and numbers in Quartus entity names. They usually correspond with filenames because one entity is stored in the file of the same filename. Its identifier must start with a letter, the last character cannot be an underscore, and two connected underscores are not allowed. However, the entity names with underscores can sometimes collapse the internal Quartus simulator. We do not find out why. It just sometimes happens. It is better to avoid underscores.

VHDL is not case-sensitive, but we should keep capitalization. If we define the symbol Data, the wrong style refers to it as "data" or "DATA".
VHDL does not understand diacritics and non-ASCII characters, not even in comments.

2. Initial Configuration

Before creating your first project, you should perform permanent global configurations that will be reflected in all the following projects.

Select **Option** from Quartus menu Tools:

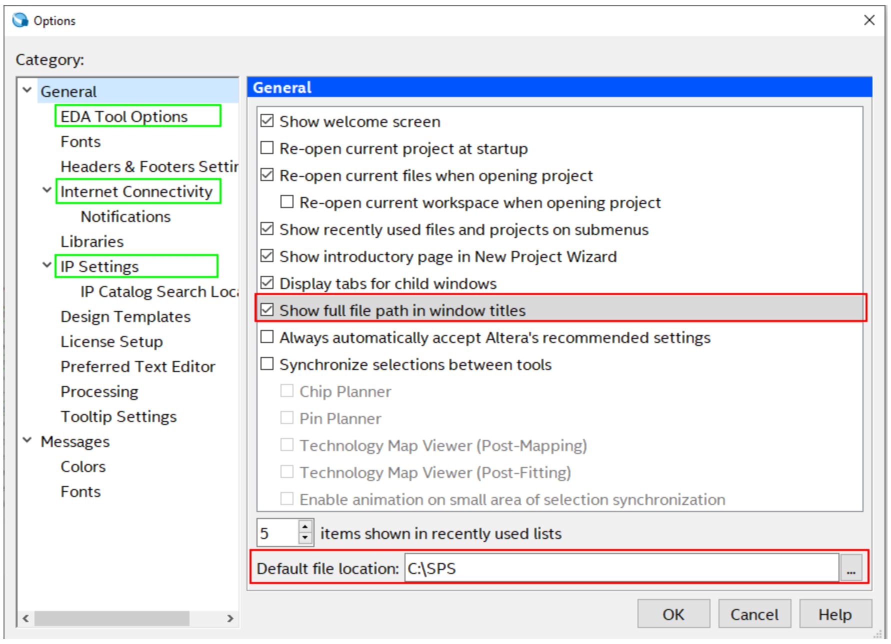

Quartus Prime Lite Edition
File Edit View Project Assignments Processing Tools Window Help
Project Navigator Hierarchy
Compilation Hierarchy
Assembler (Generate programm
Timing Analysis
All <<Filter>>
Type ID Message
System Processing
Messages
Run Simulation Tool
Launch Simulation Library Compiler
Launch Design Space Explorer II
Timing Analyzer
[redacted]
IP Catalog
Nios II Software Build Tools for Eclipse
Platform Designer
Tcl Scripts...
Customize...
Options...
License Setup...
Install Devices...

Changes user preferences and options

We begin by the General tab, specifying the default directory for storing our projects. Its choice is ours.

We recommend also checking:

"Show full file path in window titles" to improve orientation.



General

- [✓] Show welcome screen
- [ ] Re-open current project at startup
- [✓] Re-open current files when opening project
  - [ ] Re-open current workspace when opening project
- [✓] Show recently used files and projects on submenus
- [✓] Show introductory page in New Project Wizard
- [✓] Display tabs for child windows
- [✓] Show full file path in window titles
- [ ] Always automatically accept Altera's recommended settings
- [ ] Synchronize selections between tools
  - [ ] Chip Planner
  - [ ] Pin Planner
  - [ ] Technology Map Viewer (Post-Mapping)
  - [ ] Technology Map Viewer (Post-Fitting)
  - [ ] Enable animation on small area of selection synchronization

5 items shown in recently used lists

Default file location: C:\SPS

EDA Tool Options

Quartus Version 20.1

Then, we proceed to EDA Tool Options and set the path to ModelSim-Altera to ensure it will always be located.

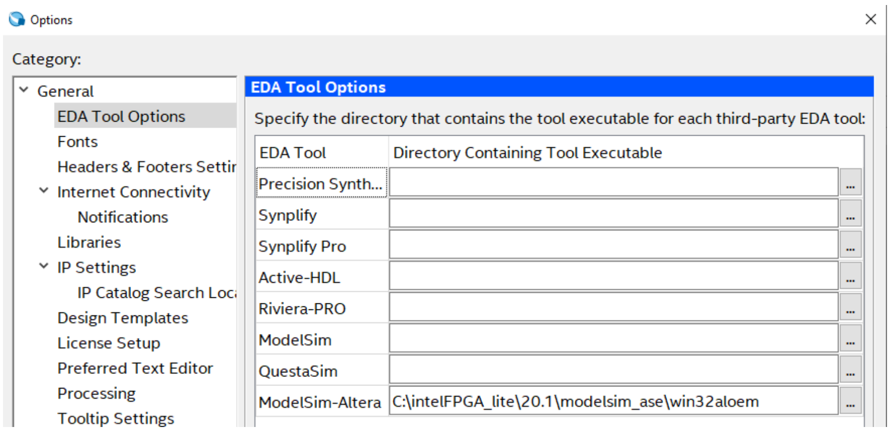
We find it in subfolder

modelsim_ase\win32aloem

of the install directory. The default is:

C:\intelFPGA_lite\20.1\

.



EDA Tool Options

Specify the directory that contains the tool executable for each third-party EDA tool:

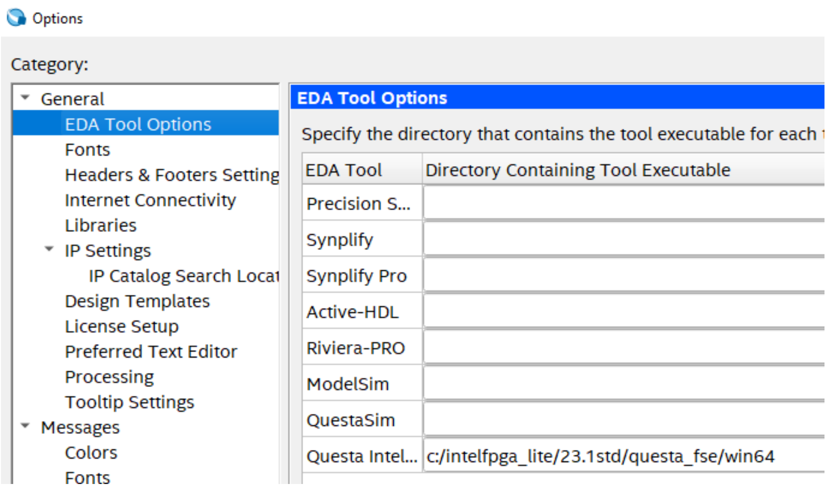
EDA Tool	Directory Containing Tool Executable
Precision Synth...	
Synplify	
Synplify Pro	
Active-HDL	
Riviera-PRO	
ModelSim	
QuestaSim	
ModelSim-Altera	C:\intelFPGA_lite\20.1\modelsim_ase\win32aloem

Quartus Version 23.1

We then go to EDA Tool Options and set the path to Intel-Questa to ensure it is always located.

It can be found in the subfolder questa_fse/win64 installation directory. The default value is: c:/intelfpga_lite/23.1std/

.

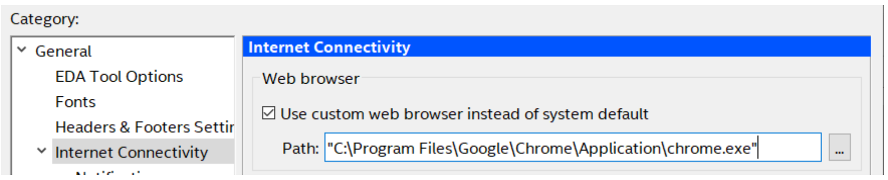


Specify the directory that contains the tool executable for each

EDA Tool	Directory Containing Tool Executable
Precision S...	
Synplify	
Synplify Pro	
Active-HDL	
Riviera-PRO	
ModelSim	
QuestaSim	
Questa Intel...	c:/intelfpga_lite/23.1std/questa_fse/win64

Note: The acronym EDA here refers to Electronic Design Automation tools that chip designers use to analyze entire semiconductor chips. The Quartus installation contains only one free tool, ModelSim Altera, i.e., ModelSim with embedded Quartus FPGA libraries, V23.1 Questa.

We can also set our default browser. Quartus uses it to display its helps.

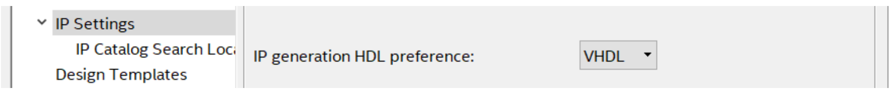


☑ Use custom web browser instead of system default

Path: "C:\Program Files\Google\Chrome\Application\chrome.exe"

In IP Setting category, select VHDL.

Note: IP is Intelligent Property here.



IP generation HDL preference: VHDL

If you wish, you can adjust the primary and message fonts and, eventually, other options.

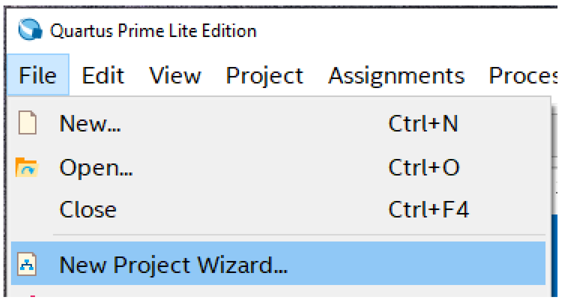
Finally, close the Option dialog by [OK] button to store changes; otherwise, the changes will be canceled.

Then, close Quartus Prime and **rerun it** so Quartus starts with new options!!!!

3. Project Wizard of the First Project

Creating our first project is complicated by many settings, but it is one one-time task; the following projects are made in a minute; see Chapter 5 on page 15.

From the main menu Quartus, we choose File-> New Project Wizard.

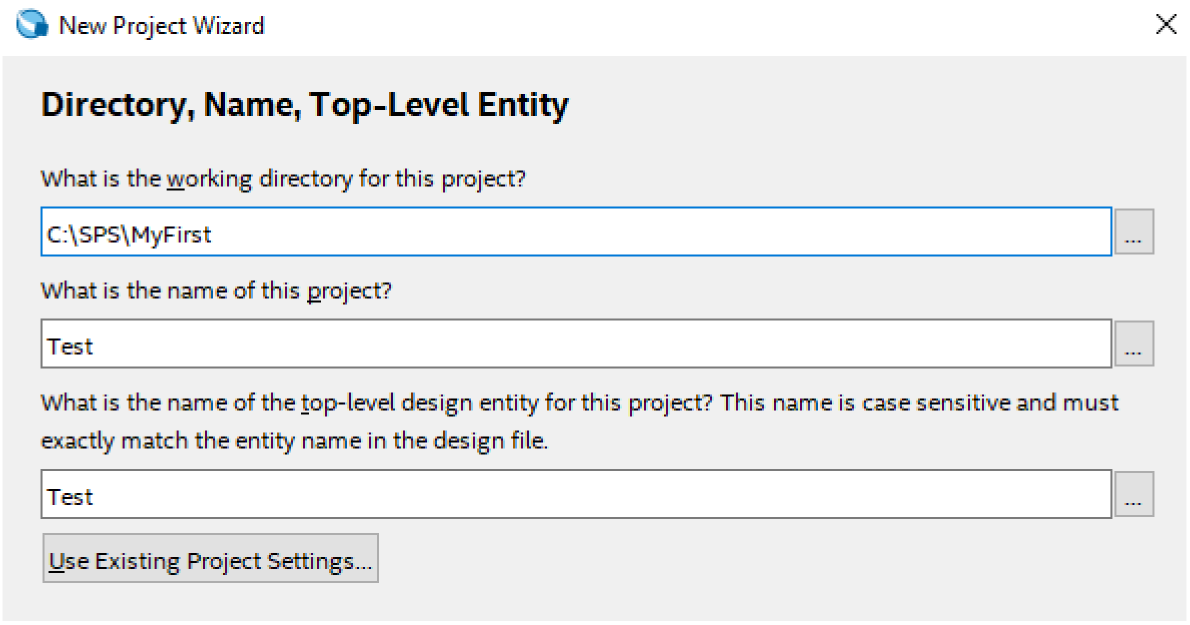

Quartus Prime Lite Edition
File Edit View Project Assignments Proces
New... Ctrl+N
Open... Ctrl+O
Close Ctrl+F4
New Project Wizard...

The Wizard's dialog consists of several pages; you can scroll from one page to another, forward by [Next], and backward by [Back].

►**Introduction** — continue by [Next >]

►**Directory, Name, Top-Level Entity**

Enter any folder name inside an existing directory, e.g., "MyFirst" — the folder should not exist yet; it will be created. We also choose names for our project and entity, e.g., "Test". Do not use anything that could accidentally be an HDL language keyword, such as "else", "input", "output", and so on.



New Project Wizard

Directory, Name, Top-Level Entity

What is the working directory for this project?

C:\SPS\MyFirst

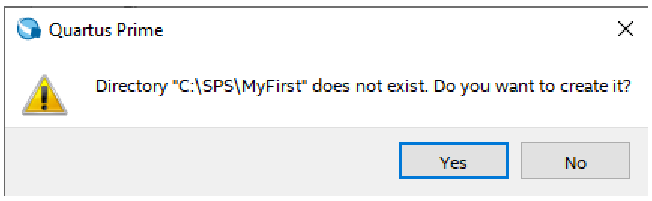
What is the name of this project?

Test

What is the name of the top-level design entity for this project? This name is case sensitive and must exactly match the entity name in the design file.

Test

After entering all items, click the [Next >] button and confirm the creation of a new directory. If you look at this question, it is a good sign that Quartus projects do not share its directories.



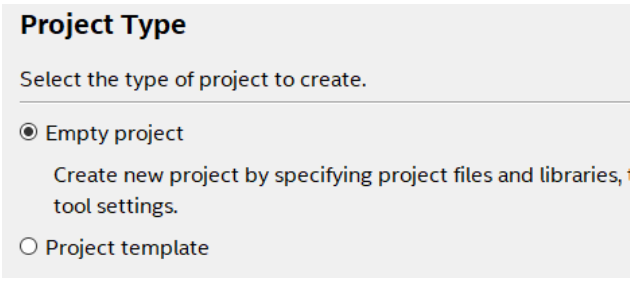
Quartus Prime

Directory "C:\SPS\MyFirst" does not exist. Do you want to create it?

Note 1: *Quartus does not allow the storage of two projects in one folder! Each project has its directory.*

Note 2: *Unlike older Quartus versions, the button [Use Existing Project Settings] does not allow copying many settings in Quartus 20.1. We show the better way on page 13.*

▶**Project Types** —We select Empty and press [Next >] because project templates do not exist for our educational board Veek-MT2.


Project Type

Select the type of project to create.

◉ Empty project

Create new project by specifying project files and libraries,
tool settings.

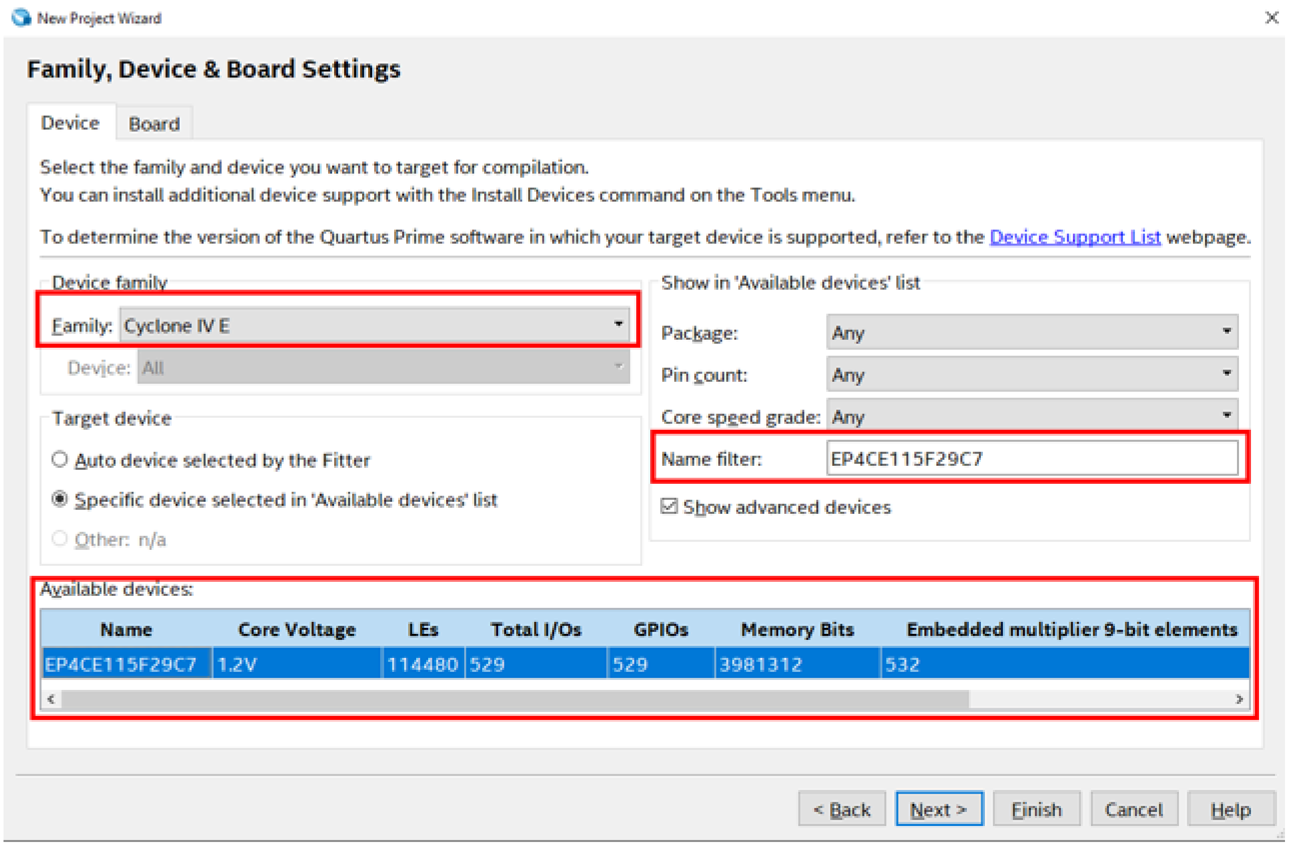
○ Project template

▶ **Add Files** - skip by [Next >]

▶**Family Device & Board Settings** —enter the following for development board Veek-MT2:

- First, we must set the family: **Cyclone IV E**
- Then, we write/copy in the name filter: **EP4CE115F29C7**

In the list of available devices, we select FPGA EP4CE115F29C7 by mouse double click.



Family, Device & Board Settings

Select the family and device you want to target for compilation.
You can install additional device support with the Install Devices command on the Tools menu.

To determine the version of the Quartus Prime software in which your target device is supported, refer to the Device Support List webpage.

Device family

Family: Cyclone IV E

Device: All

Target device

○ Auto device selected by the Fitter

◉ Specific device selected in 'Available devices' list

○ Other: n/a

Show in 'Available devices' list

Package: Any

Pin count: Any

Core speed grade: Any

Name filter: EP4CE115F29C7

☑ Show advanced devices

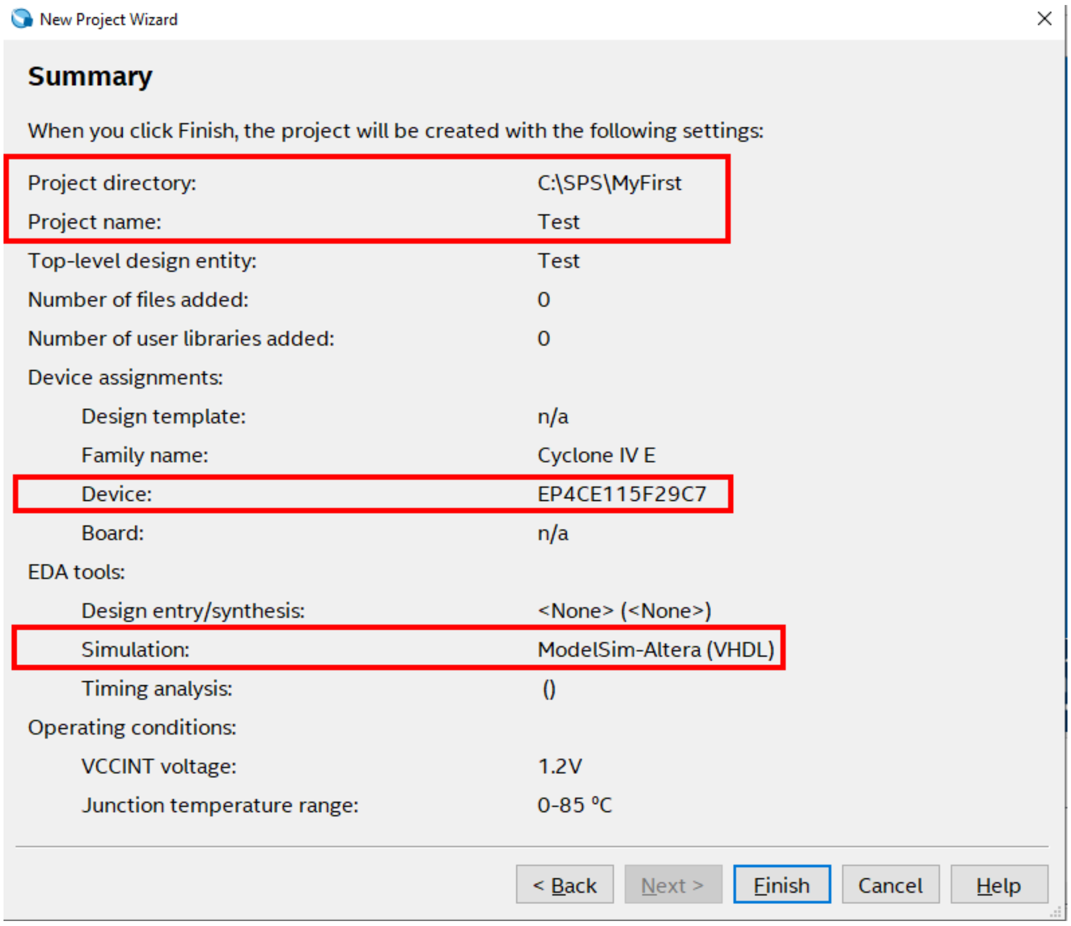
Available devices:

Name	Core Voltage	LEs	Total I/Os	GPIOs	Memory Bits	Embedded multiplier 9-bit elements
EP4CE115F29C7	1.2V	114480	529	529	3981312	532

Click [Next>]

►**Summary** – check if everything is OK.

Version Qurtus 20.1

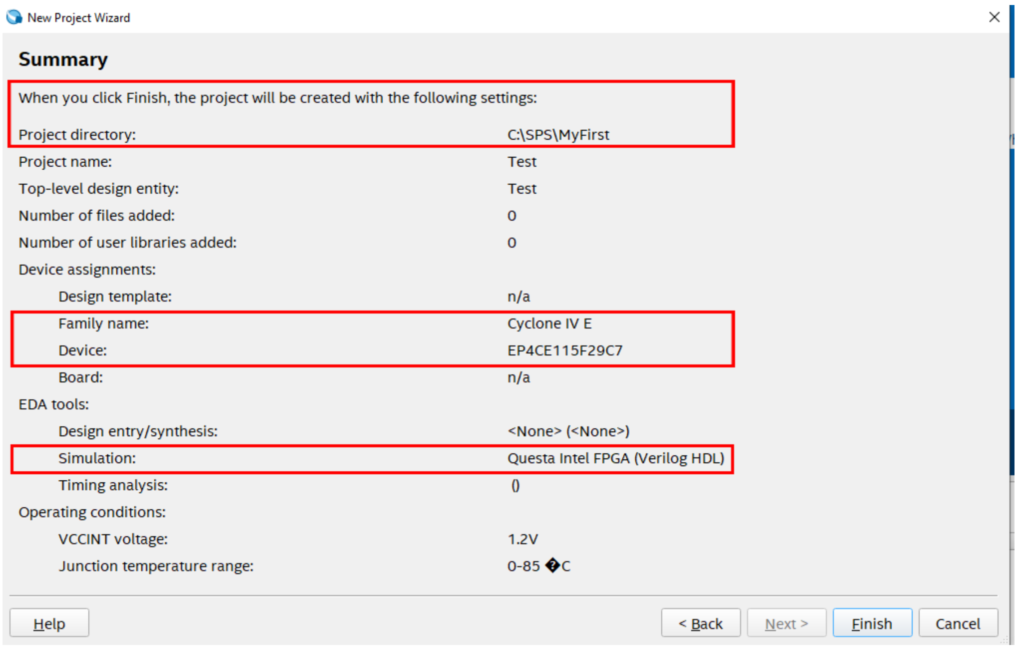


Summary

When you click Finish, the project will be created with the following settings:

Project directory:	C:\SPS\MyFirst
Project name:	Test
Top-level design entity:	Test
Number of files added:	0
Number of user libraries added:	0
Device assignments:	
Design template:	n/a
Family name:	Cyclone IV E
Device:	EP4CE115F29C7
Board:	n/a
EDA tools:	
Design entry/synthesis:	<None> (<None>)
Simulation:	ModelSim-Altera (VHDL)
Timing analysis:	()
Operating conditions:	
VCCINT voltage:	1.2V
Junction temperature range:	0-85 °C

Version Q23.1



Summary

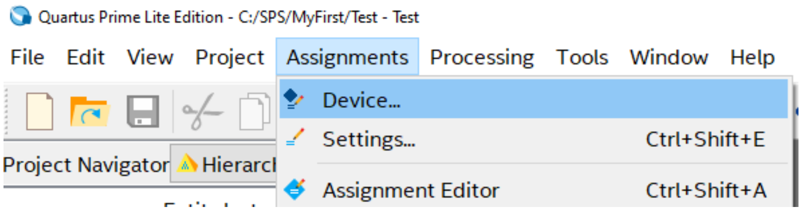
When you click Finish, the project will be created with the following settings:

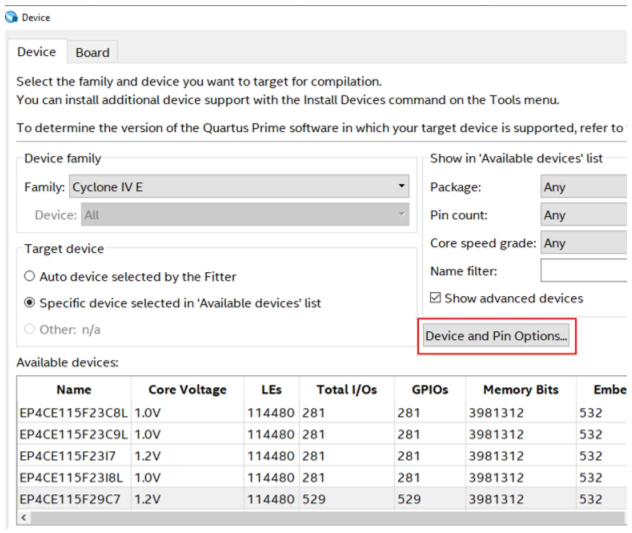
Project directory:	C:\SPS\MyFirst
Project name:	Test
Top-level design entity:	Test
Number of files added:	0
Number of user libraries added:	0
Device assignments:	
Design template:	n/a
Family name:	Cyclone IV E
Device:	EP4CE115F29C7
Board:	n/a
EDA tools:	
Design entry/synthesis:	<None> (<None>)
Simulation:	Questa Intel FPGA (Verilog HDL)
Timing analysis:	()
Operating conditions:	
VCCINT voltage:	1.2V
Junction temperature range:	0-85 �C

If it is OK, click [Finish].

3.1 Additional Project Setting for Board Veek-MT2

Open the Device dialog from the Quartus menu Assignments->Device:


Quartus Prime Lite Edition - C:/SPS/MyFirst/Test - Test
File Edit View Project Assignments Processing Tools Window Help
Device...
Settings... Ctrl+Shift+E
Assignment Editor Ctrl+Shift+A
Project Navigator
Hierarcl


Device

Device | Board

Select the family and device you want to target for compilation.
You can install additional device support with the Install Devices command on the Tools menu.

To determine the version of the Quartus Prime software in which your target device is supported, refer to

Device family

Family: Cyclone IV E

Device: All

Target device

○ Auto device selected by the Fitter

● Specific device selected in 'Available devices' list

○ Other: n/a

Show in 'Available devices' list

Package: Any

Pin count: Any

Core speed grade: Any

Name filter:

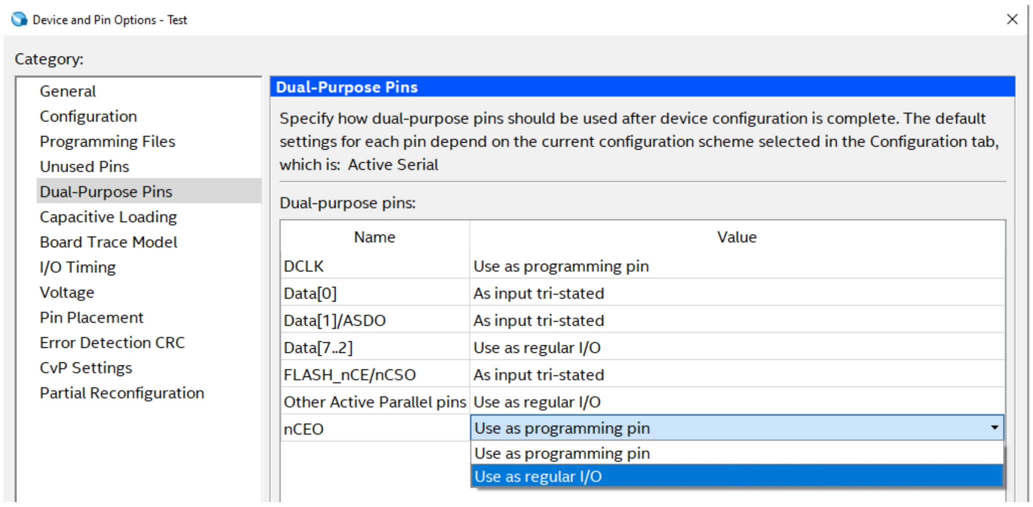
☑ Show advanced devices

Device and Pin Options...

Available devices:

Name	Core Voltage	LEs	Total I/Os	GPIOs	Memory Bits	Embe
EP4CE115F23C8L	1.0V	114480	281	281	3981312	532
EP4CE115F23C9L	1.0V	114480	281	281	3981312	532
EP4CE115F23I7	1.2V	114480	281	281	3981312	532
EP4CE115F23I8L	1.0V	114480	281	281	3981312	532
EP4CE115F29C7	1.2V	114480	529	529	3981312	532

We saw this dialog in Project Wizard, but now, the new button [Device and Pin Options] appears here. Click on it and select in the Dual-Purpose Pins tab that nCEO pin of FPGA will be used as regular I/O.


Device and Pin Options - Test

Category:

- General
- Configuration
- Programming Files
- Unused Pins
- Dual-Purpose Pins
- Capacitive Loading
- Board Trace Model
- I/O Timing
- Voltage
- Pin Placement
- Error Detection CRC
- CvP Settings
- Partial Reconfiguration

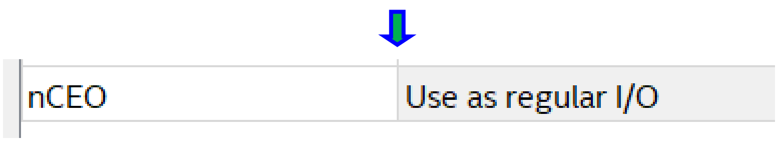
Dual-Purpose Pins

Specify how dual-purpose pins should be used after device configuration is complete. The default settings for each pin depend on the current configuration scheme selected in the Configuration tab, which is: Active Serial

Dual-purpose pins:

Name	Value
DCLK	Use as programming pin
Data[0]	As input tri-stated
Data[1]/ASDO	As input tri-stated
Data[7..2]	Use as regular I/O
FLASH_nCE/nCSO	As input tri-stated
Other Active Parallel pins	Use as regular I/O
nCEO	Use as programming pin

Use as programming pin
Use as regular I/O


nCEO | Use as regular I/O

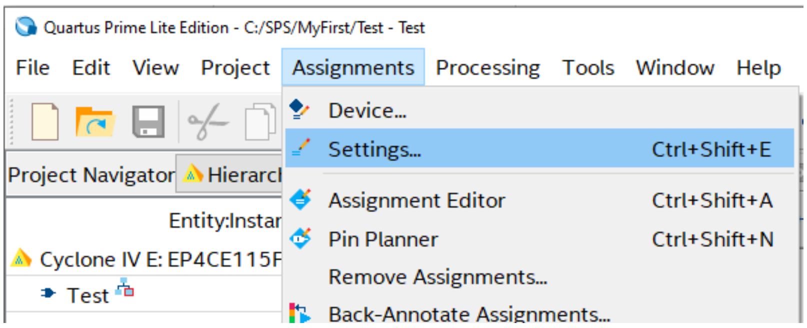
By [OK] buttons, we first close the sub dialog "Device and Pin Options" and then the "Device" dialog.

Note: Pin nCEO (Chip Enable Output) allows in JTAG communication the selection of an FPGA device, to which we download configuration.

VEEK-MT2 board contains only one FPGA chip, which is always selected, so it utilizes free nCEO *as programming pin (for LCD color bit); therefore, we must inform Quartus about nCEO modification.*

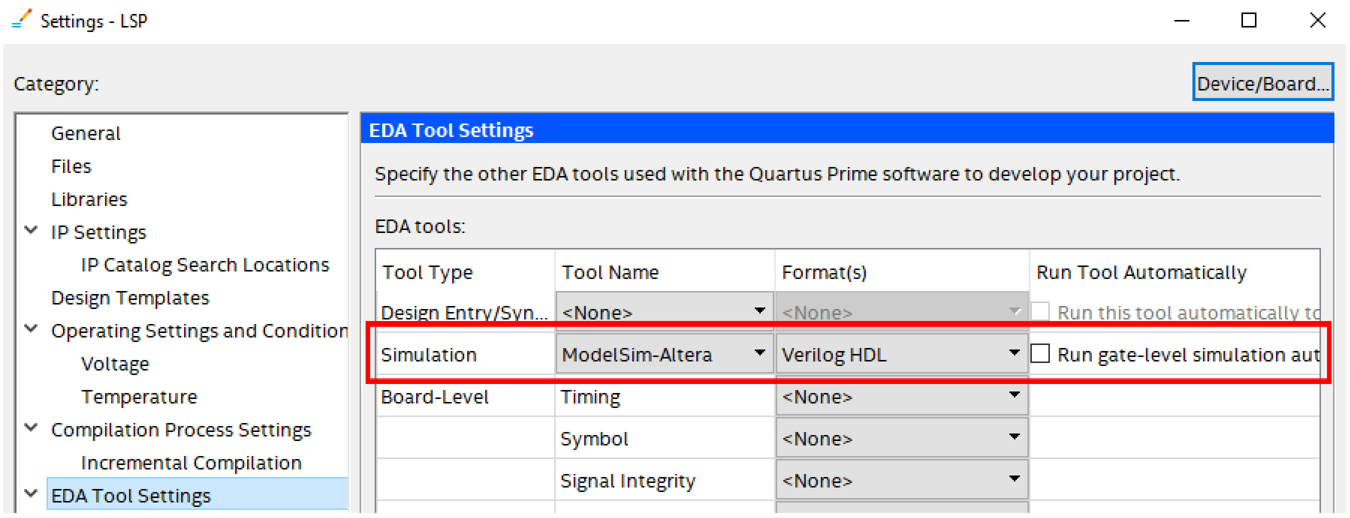
3.2 ►Setting up EDA tools

Invoke the Settings dialog from the Quartus menu:


Quartus Prime Lite Edition - C:/SPS/MyFirst/Test - Test
File Edit View Project Assignments Processing Tools Window Help
Device...
Settings... Ctrl+Shift+E
Assignment Editor Ctrl+Shift+A
Pin Planner Ctrl+Shift+N
Remove Assignments...
Back-Annotate Assignments...
Project Navigator Hierarcl
Entity:Instar
Cyclone IV E: EP4CE115F
Test

In its Category tree, select EDA Tool Settings. Set up the simulation tool to ModelSim Altera in VHDL. Do not change anything else here

Version 20.1- Set Model-Sim-Altera in VHDL and leave the other items in their default state! The free version does not contain other EDA programs.



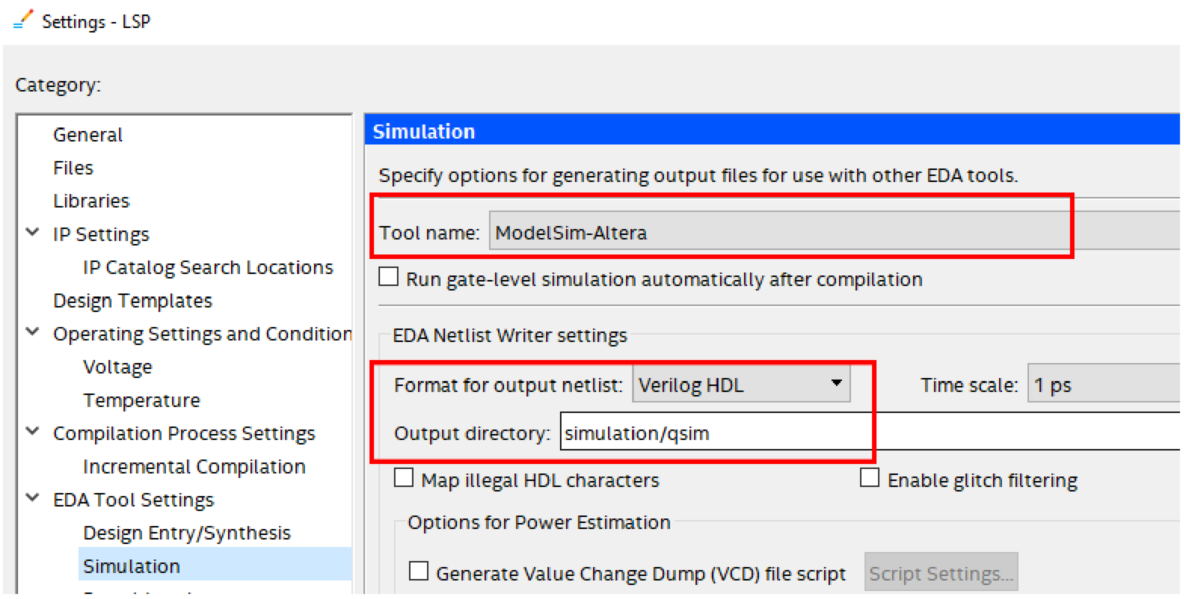
EDA Tool Settings

Specify the other EDA tools used with the Quartus Prime software to develop your project.

EDA tools:

Tool Type	Tool Name	Format(s)	Run Tool Automatically
Design Entry/Syn...	<None>	<None>	☐ Run this tool automatically to
Simulation	ModelSim-Altera	Verilog HDL	☐ Run gate-level simulation aut
Board-Level	Timing	<None>	
	Symbol	<None>	
	Signal Integrity	<None>	

Change also the simulation output directory to simulation/qsim – the internal simulator of Quartus.



Simulation

Specify options for generating output files for use with other EDA tools.

Tool name: ModelSim-Altera

☐ Run gate-level simulation automatically after compilation

EDA Netlist Writer settings

Format for output netlist: Verilog HDL   Time scale: 1 ps

Output directory: simulation/qsim

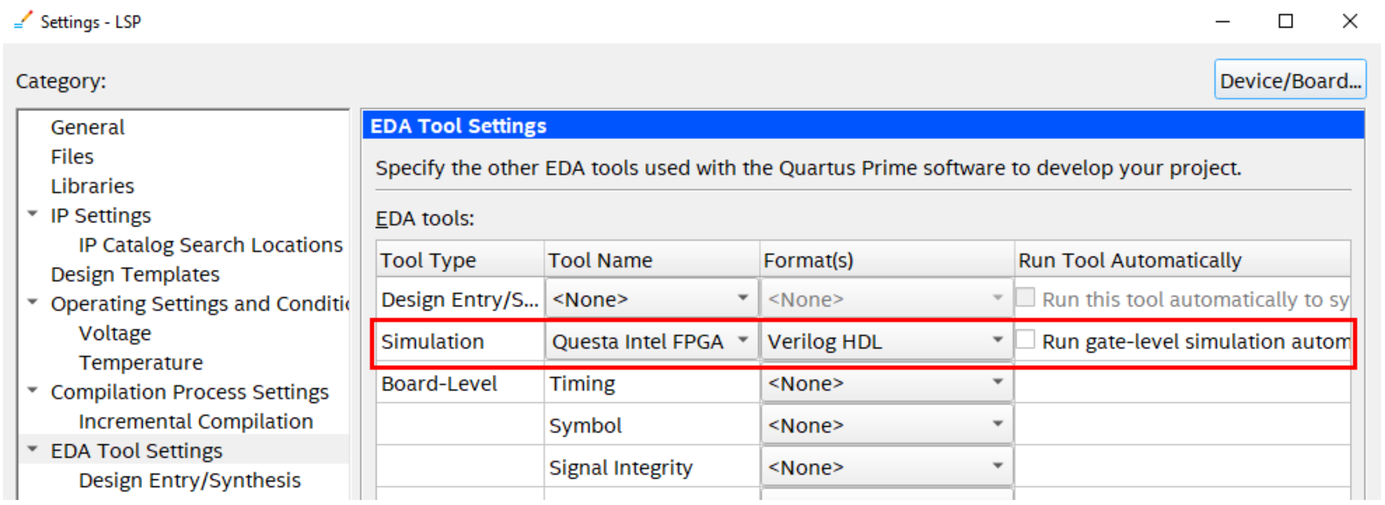
☐ Map illegal HDL characters   ☐ Enable glitch filtering

Options for Power Estimation

☐ Generate Value Change Dump (VCD) file script   Script Settings...

Version 23.1

Just make sure you have the Questa Simulator. It should appear as the default setting, if not adjust.

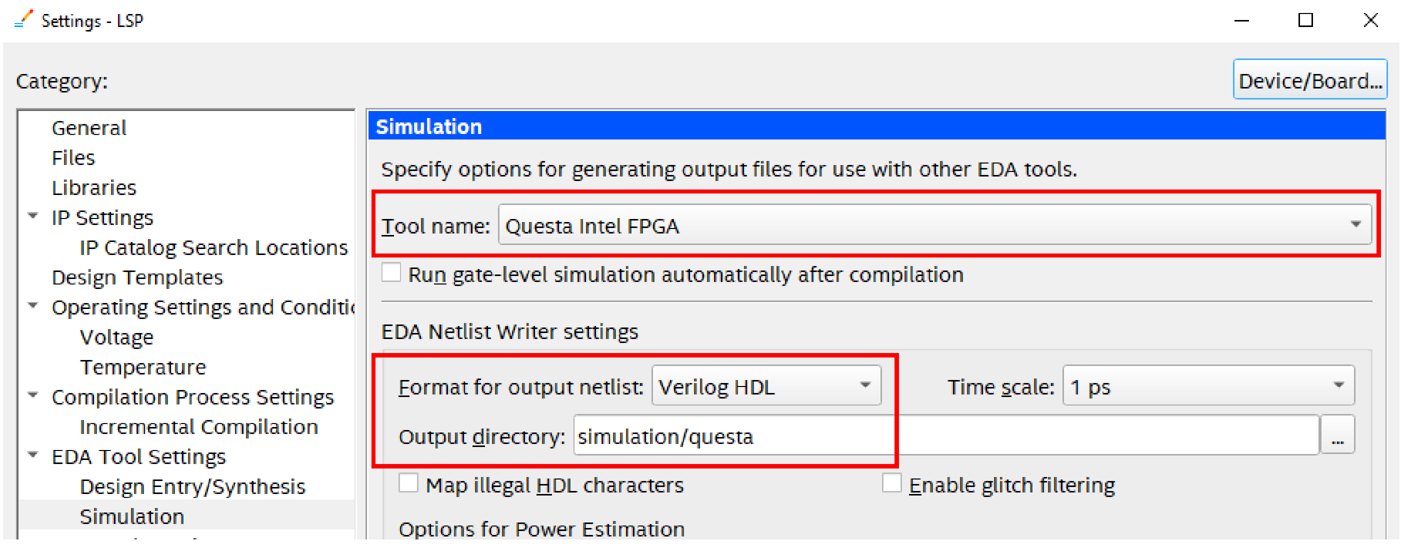


Specify the other EDA tools used with the Quartus Prime software to develop your project.

EDA tools:

Tool Type	Tool Name	Format(s)	Run Tool Automatically
Design Entry/S...	<None>	<None>	☐ Run this tool automatically to sy
Simulation	Questa Intel FPGA	Verilog HDL	☐ Run gate-level simulation autom
Board-Level	Timing	<None>	
	Symbol	<None>	
	Signal Integrity	<None>	

Check the simulation output directory; it should be to simulation/questa – the external free simulator.



Specify options for generating output files for use with other EDA tools.

Tool name: Questa Intel FPGA

☐ Run gate-level simulation automatically after compilation

EDA Netlist Writer settings

Format for output netlist: Verilog HDL

Time scale: 1 ps

Output directory: simulation/questa

☐ Map illegal HDL characters

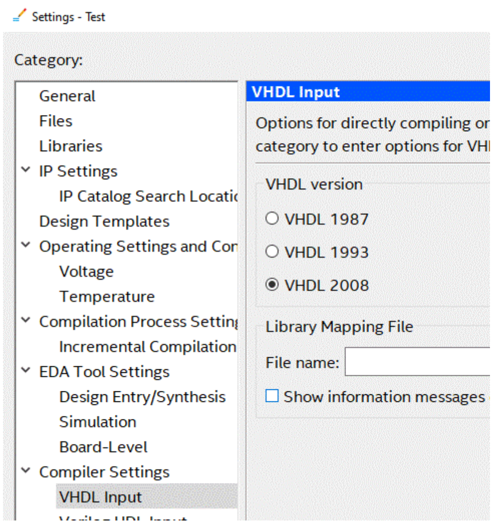
☐ Enable glitch filtering

Options for Power Estimation

Finally, we close the Setting dialog by the **[OK] button** to accept data.

3.2.a. Compiler

In the Compiler Category -> VHDL Input category, check VHDL 2008.



Options for directly compiling or category to enter options for VH

VHDL version

○ VHDL 1987

○ VHDL 1993

● VHDL 2008

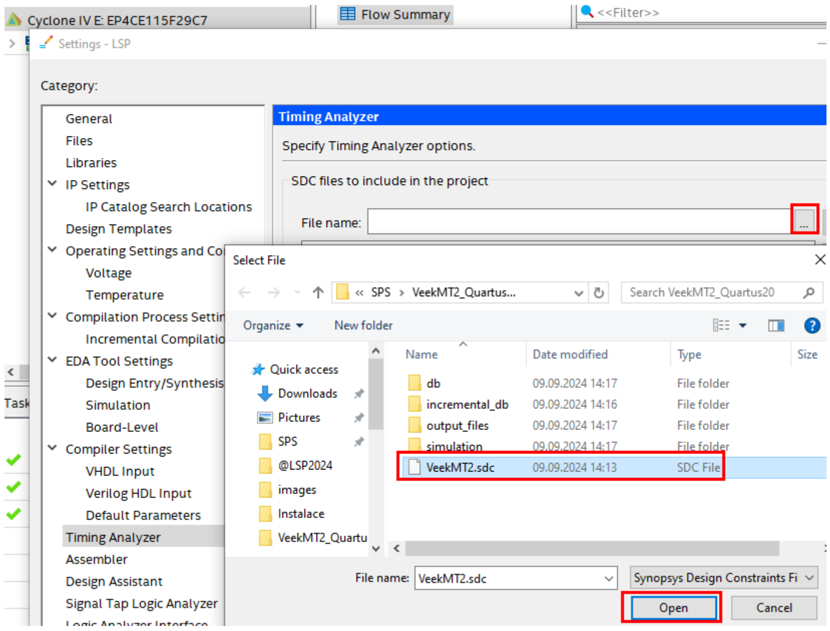
Library Mapping File

File name:

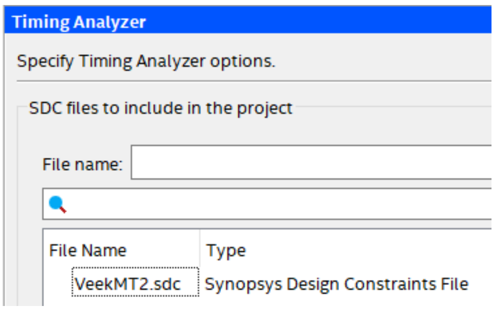
☐ Show information messages

3.3 TimeQuest Setting

From the default project, copy the VeekMT2.sdc file to the main project folder and then on the Settings dialog, in the Timing Analyzer category, look for the *.sdc file (Synopsys Design Constraints).



Add it into the Timing Analyzer constraints file list.


Timing Analyzer
Specify Timing Analyzer options.
SDC files to include in the project
File name:

File Name	Type
VeekMT2.sdc	Synopsys Design Constraints File

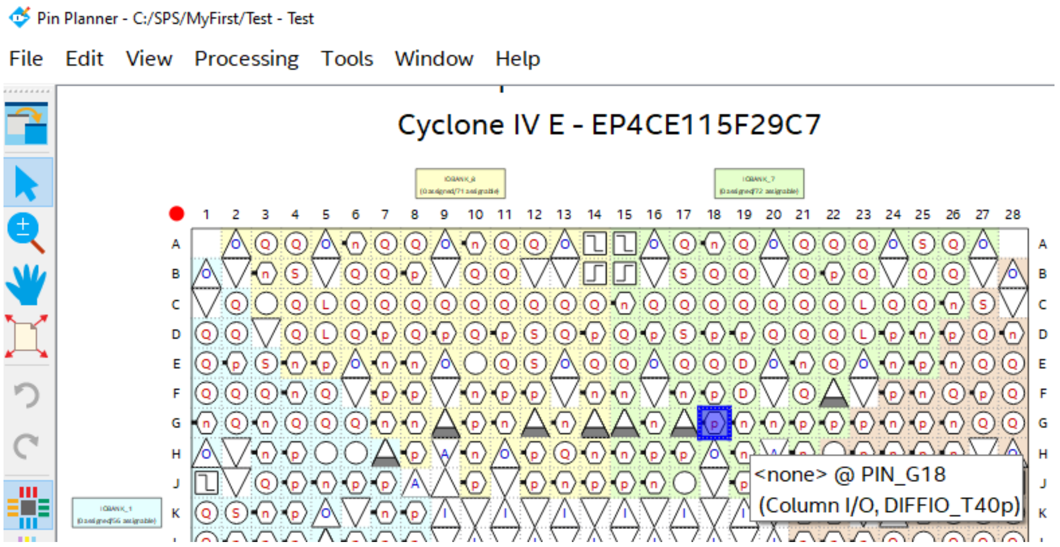
*Note: The *.sdc files inform Quartus that the VEEK-MT2 teaching board contains a 50 MHz clock generator. The clock frequency is a critical specification. Without this information, our circuit will be built for a default frequency of 1 GHz. The internal circuitry of FPGAs depends on the frequency, as we explain in our lectures, so the result will be non-functional.*

Finally, close the Settings dialog box with **[OK] and** accept the data.

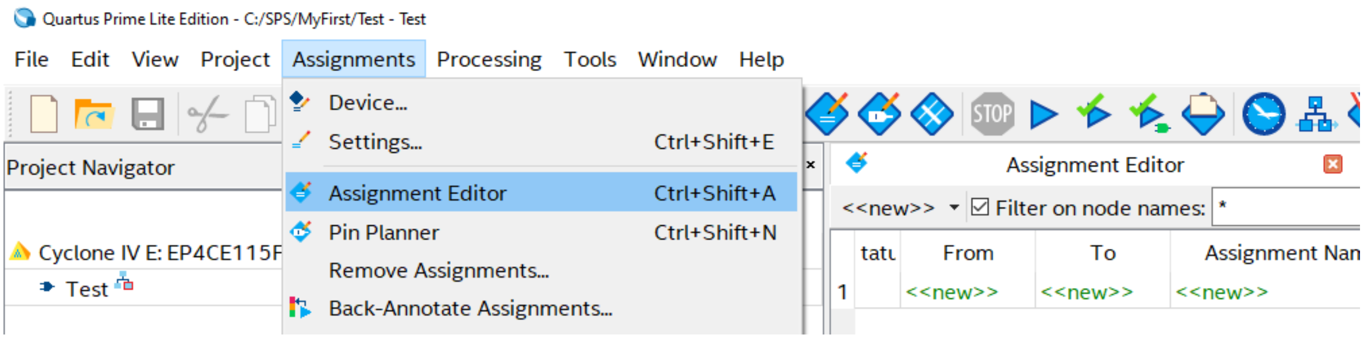
3.4 Pin Assignments

FPGA chip used in VEEK-MT2 has 780 solder balls arranged in a grid or array at the bottom of the package body for external electrical connections; see the left picture [source Intel]. Each solder ball is internally one pin.

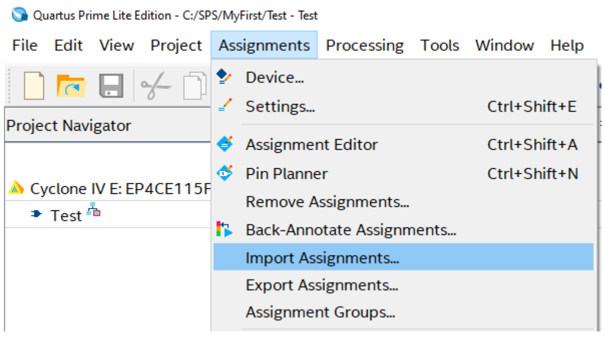
Users can direct inputs or outputs of their circuit designs up to 528 pins. This possibility can simplify printed board designs. The pins are indexed with a letter and a number. We can see them in Pin Planner.


Pin Planner - C:/SPS/MyFirst/Test - Test
File Edit View Processing Tools Window Help
Cyclone IV E - EP4CE115F29C7
<none> @ PIN_G18
(Column I/O, DIFFIO_T40p)

We work with a ready-made board; therefore, we must follow their placement by loading the manufacturer's pin assignments. Their absence is a frequent error in beginner's designs. Always check if the Assignment Editor shows pins and not an empty list as below:

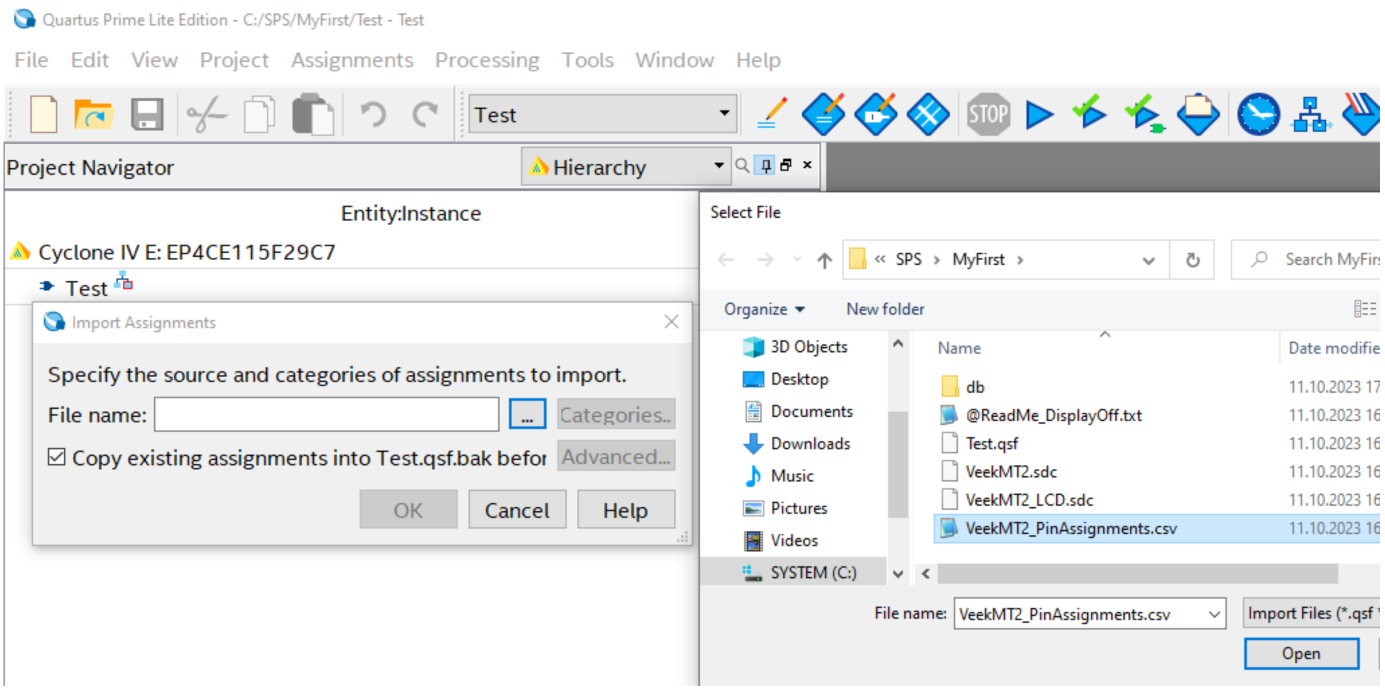

Quartus Prime Lite Edition - C:/SPS/MyFirst/Test - Test
File Edit View Project Assignments Processing Tools Window Help
Device...
Settings... Ctrl+Shift+E
Assignment Editor Ctrl+Shift+A
Pin Planner Ctrl+Shift+N
Remove Assignments...
Back-Annotate Assignments...
Project Navigator
Cyclone IV E: EP4CE115F
Test
Assignment Editor
<<new>> Filter on node names: *
tatu From To Assignment Nan
1 <<new>> <<new>> <<new>>

The original pin indexes are complex to remember, so we import their association with their symbolic names defined by the Pin Assignment spreadsheet table. In the main Quartus menu, select: **Assignments->Import Assignments.**



From the default Quartus project, copy VeekMT2_PinAssignments.csv to your Quartus project root folder.

In the Import Assignment dialog, browse for the copied file VeekMT2_PinAssignments.csv.



Import Assignments

Specify the source and categories of assignments to import.

File name: [ ] ... Categories..

☑ Copy existing assignments into Test.qsf.bak befor Advanced...

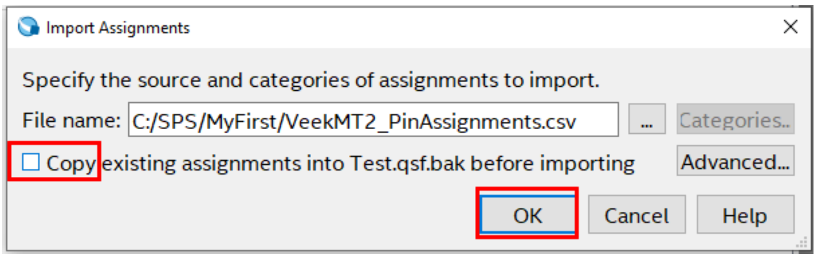
OK Cancel Help

Name	Date modifie
db	11.10.2023 17
@ReadMe_DisplayOff.txt	11.10.2023 16
Test.qsf	11.10.2023 16
VeekMT2.sdc	11.10.2023 16
VeekMT2_LCD.sdc	11.10.2023 16
VeekMT2_PinAssignments.csv	11.10.2023 16

File name: VeekMT2_PinAssignments.csv Import Files (*.qsf

We confirm the choice by [Open] and then [OK] buttons.

We have no assignment yet, so we unchecked the copy option. We import by [OK].



Import Assignments

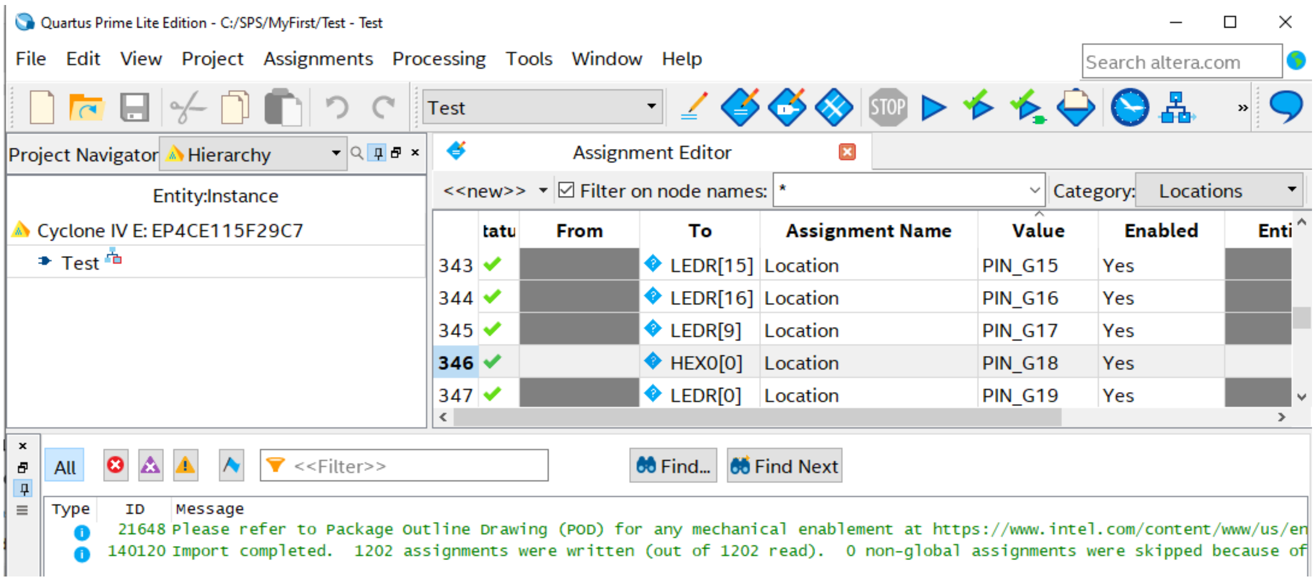
Specify the source and categories of assignments to import.

File name: C:/SPS/MyFirst/VeekMT2_PinAssignments.csv ... Categories..

☐ Copy existing assignments into Test.qsf.bak before importing Advanced...

OK Cancel Help

If we look at **Assignments-> Assignment Editor**, the list now contains associations. We can find out that PIN_G18 from the previous pin planner figure was named HEX0[0], i.e., it is the upper led segment in the least significant 7-segment digit :-)


Quartus Prime Lite Edition - C:/SPS/MyFirst/Test - Test
File Edit View Project Assignments Processing Tools Window Help
Search altera.com
Test
Project Navigator
Hierarchy
Entity:Instance
Cyclone IV E: EP4CE115F29C7
Test
Assignment Editor
All
<<Filter>>
Find...
Find Next

<<new>> ☑ Filter on node names: * Category: Locations

	tatu	From	To	Assignment Name	Value	Enabled	Enti
343	✓		LEDR[15]	Location	PIN_G15	Yes	
344	✓		LEDR[16]	Location	PIN_G16	Yes	
345	✓		LEDR[9]	Location	PIN_G17	Yes	
346	✓		HEX0[0]	Location	PIN_G18	Yes	
347	✓		LEDR[0]	Location	PIN_G19	Yes	

```
Type  ID     Message
      21648 Please refer to Package Outline Drawing (POD) for any mechanical enablement at https://www.intel.com/content/www/us/en
      140120 Import completed.  1202 assignments were written (out of 1202 read).  0 non-global assignments were skipped because of
```

<u>**It was the last setting. We have our first project.**</u>

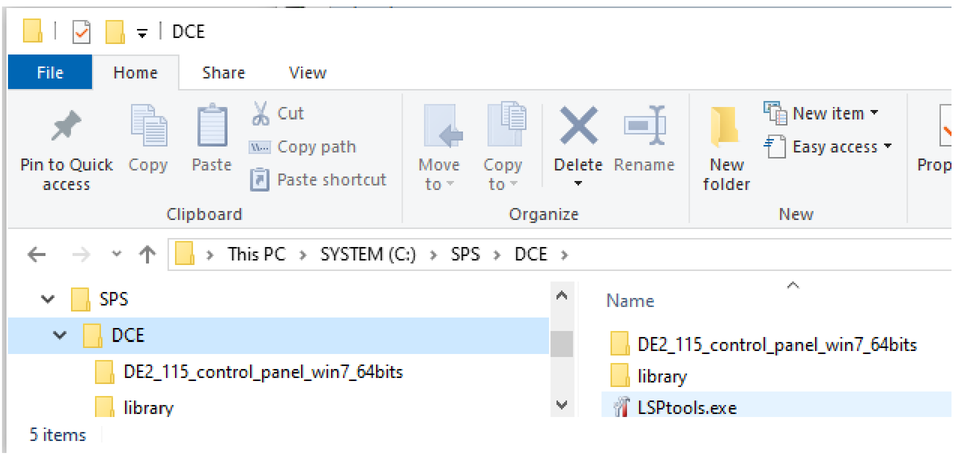
~ o ~

Never edit the pin assignment list; keep compatibility by using predefined names!

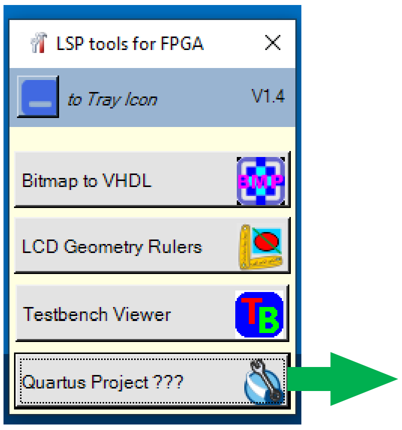
4. Checking your Project

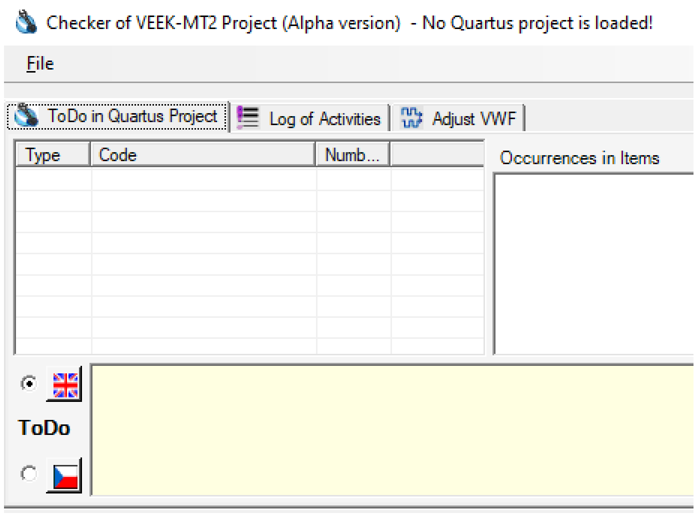
Quartus projects require many settings that are easy to make mistakes in.

Richard Šusta, the teacher of the LSP course in Dept. of Control Eng., CTU-FEE in Prague, created the LSPTools program, which includes the project verifier in Quartus. It is open source and will soon be hosted on GitHub. **Run LSPtools**:

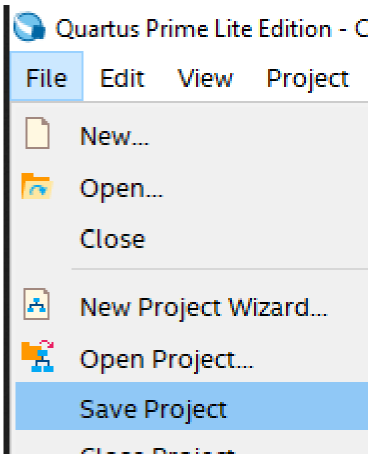


Select [Quartus Project ????] in the main windows to start the project checker.

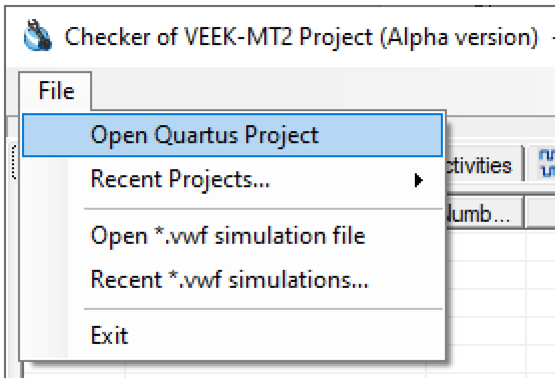




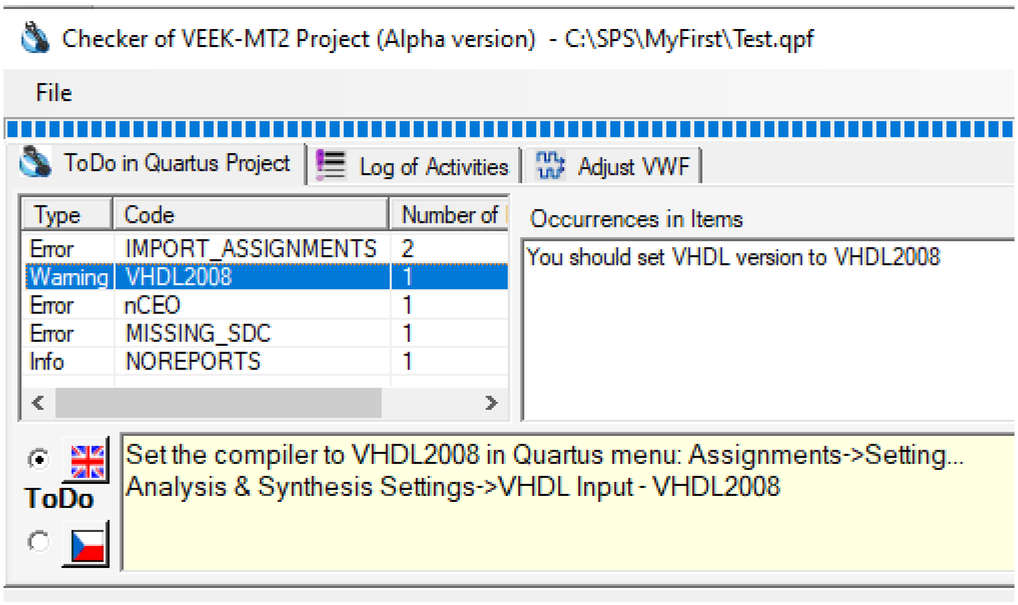
In Quartus, save the project so the checker can read its actual settings.



And open the project from the checker without closing it in Quartus.


Checker of VEEK-MT2 Project (Alpha version)
File
Open Quartus Project
Recent Projects...
Open *.vwf simulation file
Recent *.vwf simulations...
Exit

We will see it all in the reports if we have forgotten something. The picture below shows the check result of the previously correct project, now intentionally modified to demonstrate the checker. Clicking on the reports, we see help on how to remove them



Type	Code	Number of
Error	IMPORT_ASSIGNMENTS	2
Warning	VHDL2008	1
Error	nCEO	1
Error	MISSING_SDC	1
Info	NOREPORTS	1

You should set VHDL version to VHDL2008

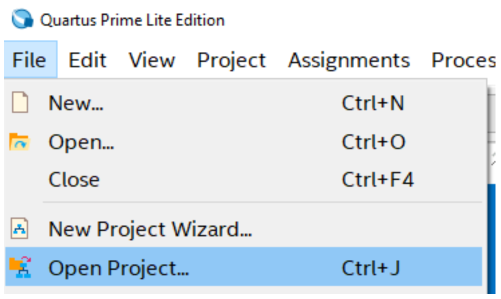
Set the compiler to VHDL2008 in Quartus menu: Assignments->Setting... Analysis & Synthesis Settings->VHDL Input - VHDL2008

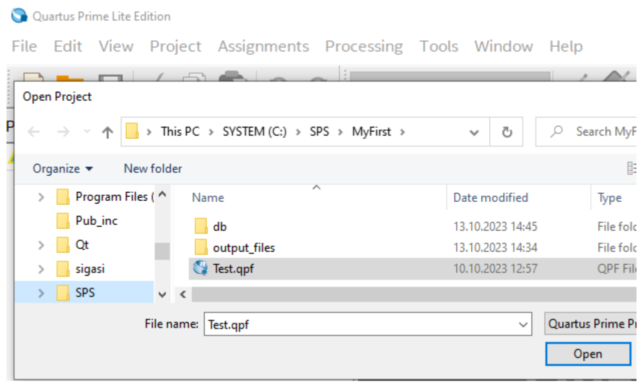
We perform corrections, save the project, and recheck it until all errors and warnings disappear.
Note: Type NOREPORTS belongs to an information message that the project does not contain compilation results, so their analysis could be performed.

5. The Express Copy of a Created Project

If I have already created at least one complete project from scratch, we can copy it to obtain another project in a minute.

From the Quartus menu, we open any of our projects, e.g., we use MyFirst:

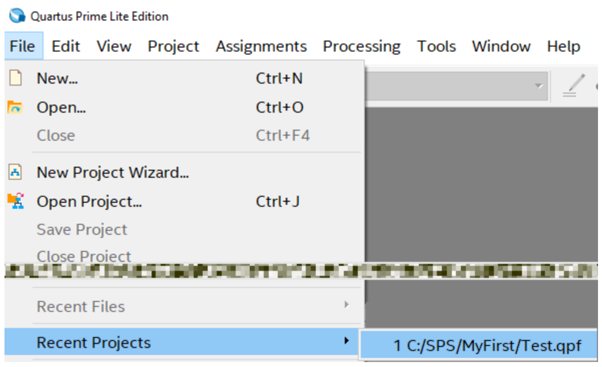



Quartus Prime Lite Edition
File Edit View Project Assignments Processing Tools Window Help
Open Project
This PC > SYSTEM (C:) > SPS > MyFirst >
Search MyF
Organize New folder
Program Files (
Pub_inc
Qt
sigasi
SPS
Open

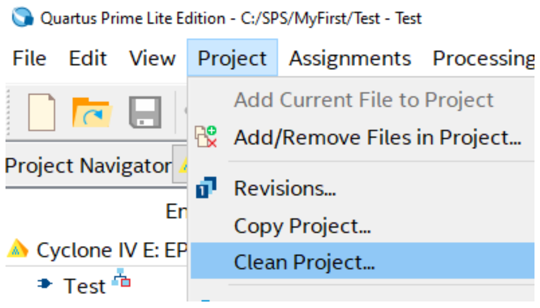
Name	Date modified	Type
db	13.10.2023 14:45	File folc
output_files	13.10.2023 14:34	File folc
Test.qpf	10.10.2023 12:57	QPF Fil

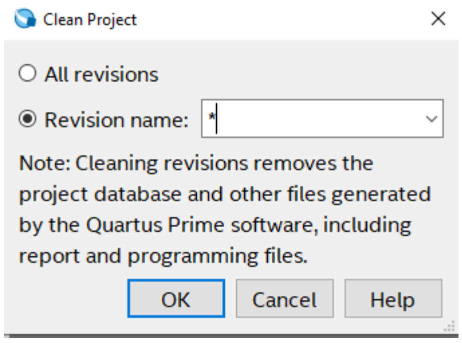
File name: Test.qpf — Quartus Prime P

Eventually, we can access it from the "Recent Project" offer:



First, we select "Project-> Clean project" to remove all temporary files, and by [OK], we confirm either the default option or All revisions.

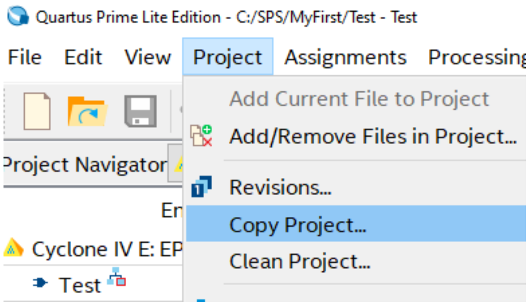

Quartus Prime Lite Edition - C:/SPS/MyFirst/Test - Test
File Edit View Project Assignments Processing
Add Current File to Project
Add/Remove Files in Project...
Revisions...
Copy Project...
Clean Project...
Project Navigator
En
Cyclone IV E: EP
Test

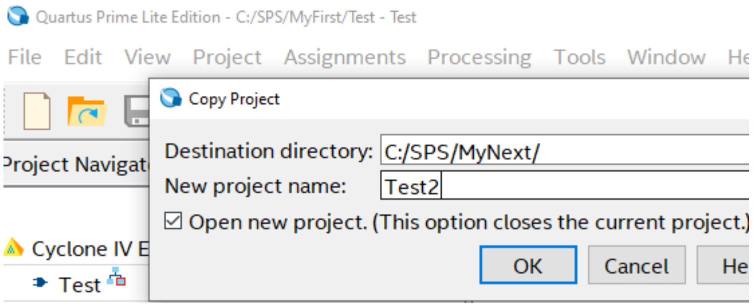


All revisions [✓ Revision name: *]

Note: Cleaning revisions removes the project database and other files generated by the Quartus Prime software, including report and programming files.

Then, we open the "Project->Copy Project" dialog. We enter our project name, e.g., Test2, and specify a directory where we want to store its files.


Quartus Prime Lite Edition - C:/SPS/MyFirst/Test - Test
File Edit View Project Assignments Processing
Add Current File to Project
Add/Remove Files in Project...
Revisions...
Copy Project...
Clean Project...
Project Navigator
En
Cyclone IV E: EP
Test

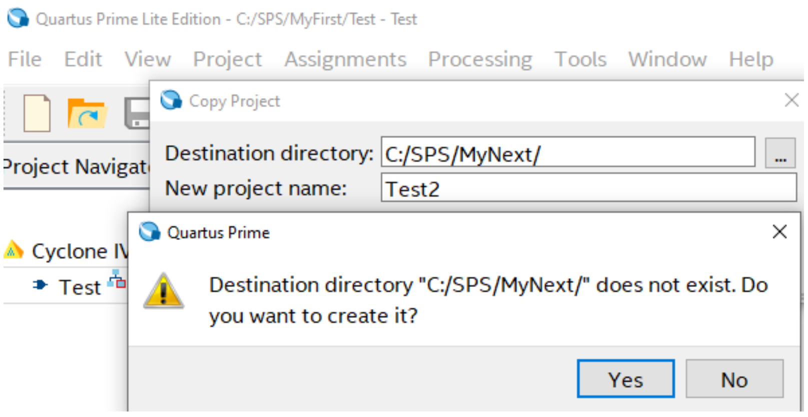

Quartus Prime Lite Edition - C:/SPS/MyFirst/Test - Test
File Edit View Project Assignments Processing Tools Window He
Copy Project
OK
Cancel
He
Project Navigat
Cyclone IV E
Test

Destination directory: C:/SPS/MyNext/

New project name: Test2

☑ Open new project. (This option closes the current project.)

After confirming our choice by [OK], the message below signals that we are creating our project in the new directory, which will be its own, as required.


Quartus Prime Lite Edition - C:/SPS/MyFirst/Test - Test
File Edit View Project Assignments Processing Tools Window Help
Project Navigat
Cyclone IV
Test
Copy Project

Destination directory: C:/SPS/MyNext/
New project name: Test2

Quartus Prime

Destination directory "C:/SPS/MyNext/" does not exist. Do you want to create it?

We have already created our new project with all the necessary settings. It also contains all the Test project files.

The following chapter explains how

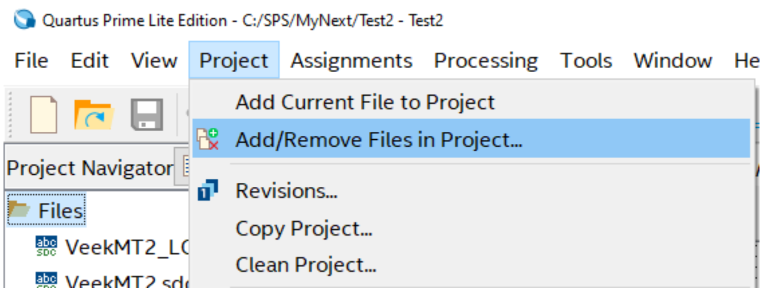
- to change Top-Level Entity;
- to adjust our project by adding new files or removing unused ones;
- to move our project to another directory or computer;
- to change the compilation result file name.

6. Working with Projects

The following steps are more adjustments than requirements.

6.1 Reorganizing files in Project Navigator

From the file dialog, we can reorganize files in our project.


Quartus Prime Lite Edition - C:/SPS/MyNext/Test2 - Test2
File Edit View Project Assignments Processing Tools Window He
Add Current File to Project
Add/Remove Files in Project...
Revisions...
Copy Project...
Clean Project...
Project Navigator
Files
VeekMT2_LC
VeekMT2.sdc

It is possible to add new files or remove ones no longer needed. The changes are performed only in the list. Files are not deleted from the hard drive; any file explorer can do it.

We always keep all our design files in the directory of the project. We easily recognize wrongly placed items by their extra path.

In the left figure, wrongly located files are marked by red box.

The first one

../MyFirst/DisplayOff.vhd

is in the parent's subfolder:

C:/SPS/MyFirst/DisplayOff.vhd

i.e., outside our project.

The second file

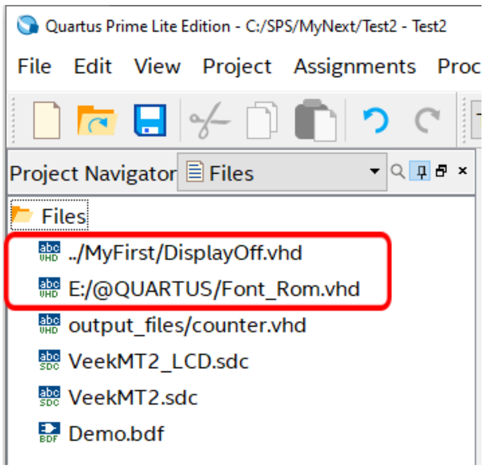
E:/@QUARTUS/Font_Rom.vhd

is stored even on a different drive.

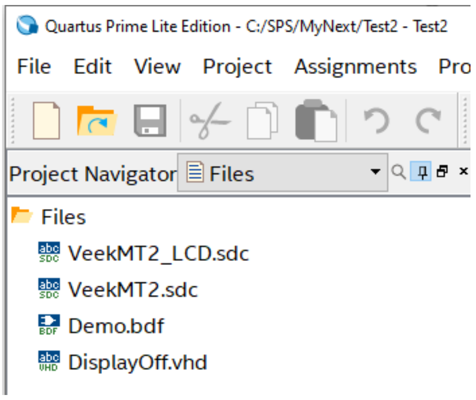
The third file

counter.vhd

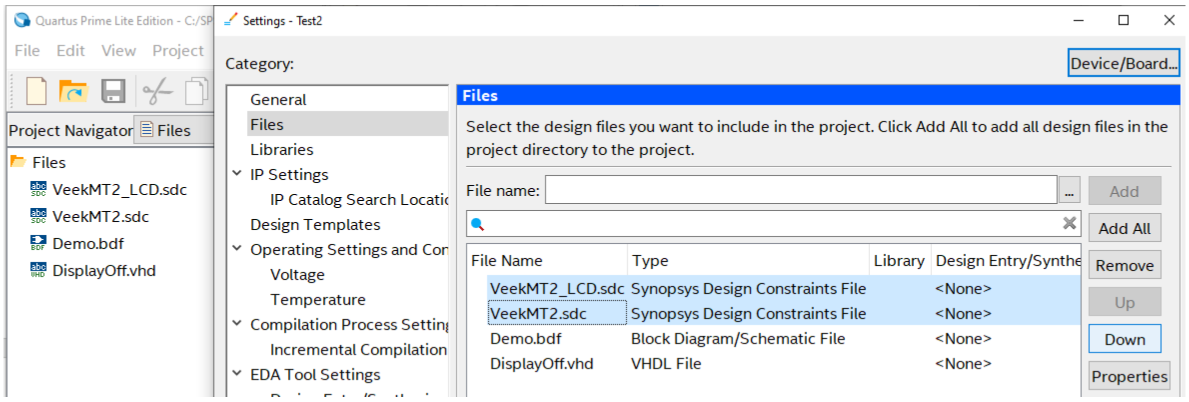
is in a subfolder output_files of our project. It is acceptable but not recommended for small projects.


Quartus Prime Lite Edition - C:/SPS/MyNext/Test2 - Test2
File Edit View Project Assignments Proc
Project Navigator
Files
Files
../MyFirst/DisplayOff.vhd
E:/@QUARTUS/Font_Rom.vhd
output_files/counter.vhd
VeekMT2_LCD.sdc
VeekMT2.sdc
Demo.bdf

The preferable file locations are in the project directory, i.e., without paths.


Quartus Prime Lite Edition - C:/SPS/MyNext/Test2 - Test2
File Edit View Project Assignments Pro
Project Navigator
Files
Files
VeekMT2_LCD.sdc
VeekMT2.sdc
Demo.bdf
DisplayOff.vhd

Eventually, we can rearrange the Project Navigator list with buttons [Up] or [Down]. Then, we confirm the changes by clicking [OK] button.



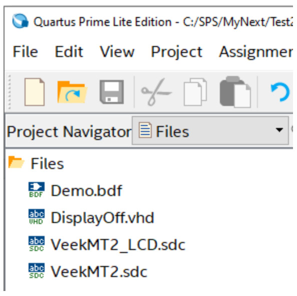
Files
- VeekMT2_LCD.sdc
- VeekMT2.sdc
- Demo.bdf
- DisplayOff.vhd

Files

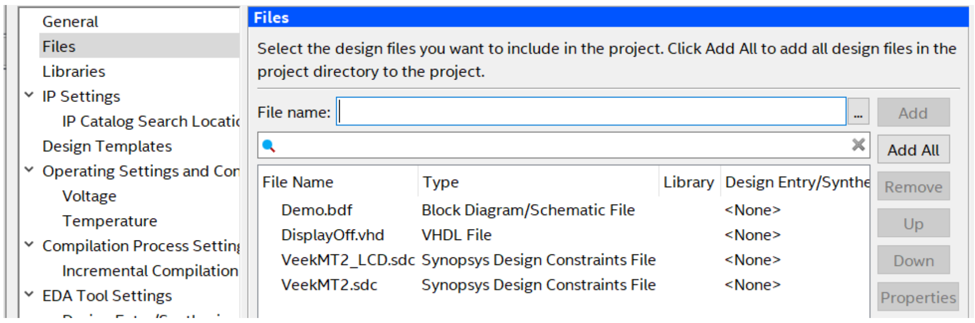
Select the design files you want to include in the project. Click Add All to add all design files in the project directory to the project.

File name:

File Name	Type	Library	Design Entry/Synthe
VeekMT2_LCD.sdc	Synopsys Design Constraints File		<None>
VeekMT2.sdc	Synopsys Design Constraints File		<None>
Demo.bdf	Block Diagram/Schematic File		<None>
DisplayOff.vhd	VHDL File		<None>


Quartus Prime Lite Edition - C:/SPS/MyNext/Test2
File Edit View Project Assignmer
Project Navigator Files

Files
- Demo.bdf
- DisplayOff.vhd
- VeekMT2_LCD.sdc
- VeekMT2.sdc



Files

Select the design files you want to include in the project. Click Add All to add all design files in the project directory to the project.

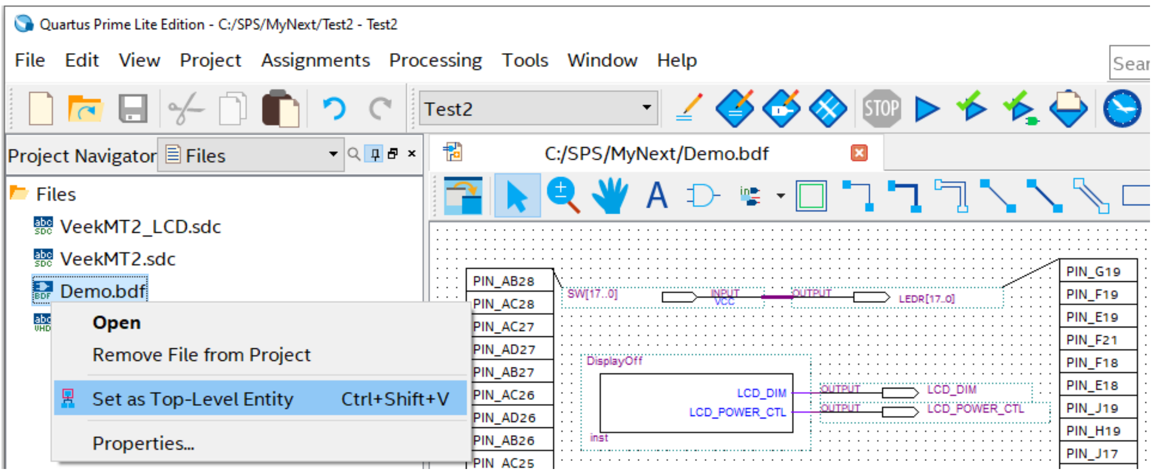
File name:

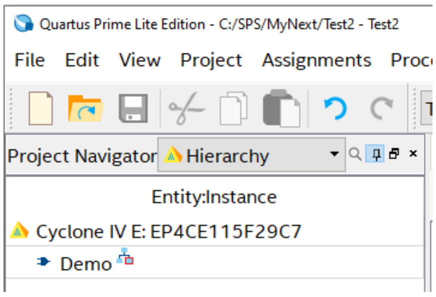
File Name	Type	Library	Design Entry/Synthe
Demo.bdf	Block Diagram/Schematic File		<None>
DisplayOff.vhd	VHDL File		<None>
VeekMT2_LCD.sdc	Synopsys Design Constraints File		<None>
VeekMT2.sdc	Synopsys Design Constraints File		<None>

6.2 *How to specify Top-Level Entity*

Our Top-Level Entity selects the design file from which the compilation begins. After we write down some synthesis files, we can dedicate anyone as the Top-Level Entity from the Project Navigator Files.

For instance, we add DisplayOff.vhd, extracted from the zip mentioned in Chapter 3.3 on page 10, and create a simple Demo.bdf that copies slider switches to red LEDs. Then, we mark it as a Top-Level entity from its context menu (a right mouse click on file).




Quartus Prime Lite Edition - C:/SPS/MyNext/Test2 - Test2
File Edit View Project Assignments Proc
Project Navigator Hierarchy
Entity:Instance
Cyclone IV E: EP4CE115F29C7
Demo

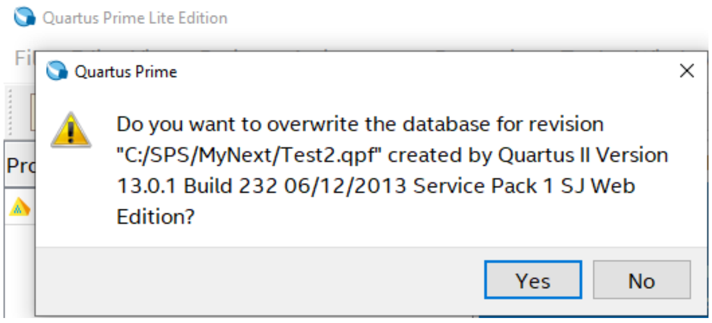
If we switch Project Navigator to the Hierarchy tab, we see that Demo has become our Top-Level Entity.

6.3 *Moving and zipping our project*

Quartus is very versatile. We can open a project created in version 20.1 in some of its previous versions, e.g., in Quartus 13.1, and any lower version project in upper Quartus.

If we have all files in the project directory, as was explained in the previous chapter, Quartus keeps their path relative. So we can rename the project's root directory or move it to another location.

When we move our project to a different computer, directory, or Quartus version, we can see a message similar to the picture below:


Quartus Prime Lite Edition

Quartus Prime

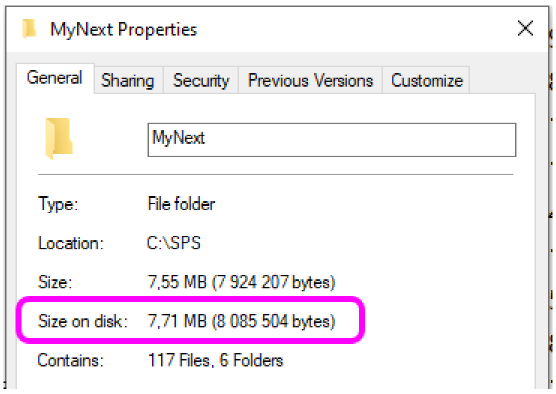
Do you want to overwrite the database for revision "C:/SPS/MyNext/Test2.qpf" created by Quartus II Version 13.0.1 Build 232 06/12/2013 Service Pack 1 SJ Web Edition?

We should always confirm [YES] if we have a small project.

Note: Compiling huge industrial designs can sometimes last for several hours. Therefore, the Quartus asks if we allow deleting previous results. It is better to let the Quartus begin with clean intermediate databases in small projects.

However, our tiny project can surprisingly contain many temporary files created during compilation and placement into an FPGA chip; see the figure below.

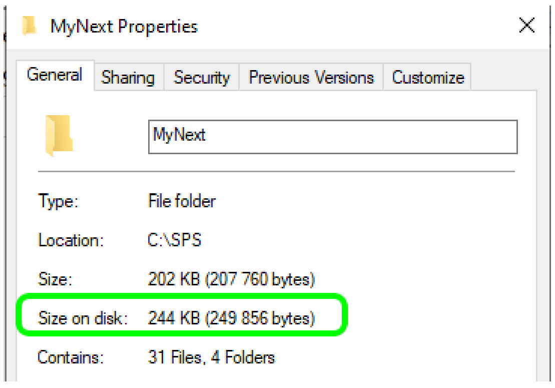
The project with Quartus compiler temporary files


MyNext Properties

MyNext

Type:	File folder
Location:	C:\SPS
Size:	7,55 MB (7 924 207 bytes)
Size on disk:	7,71 MB (8 085 504 bytes)
Contains:	117 Files, 6 Folders

without the Quartus compiler temporary file

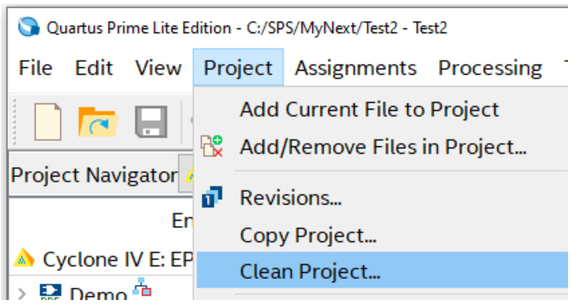

MyNext Properties

MyNext

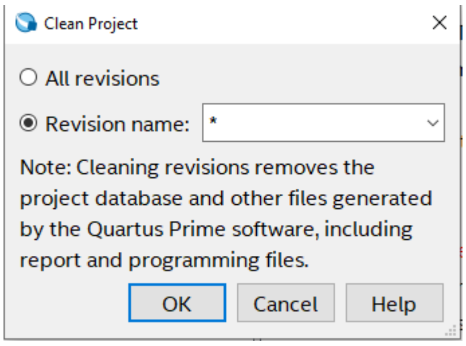
Type:	File folder
Location:	C:\SPS
Size:	202 KB (207 760 bytes)
Size on disk:	244 KB (249 856 bytes)
Contains:	31 Files, 4 Folders

Even if our design had a few files, the FPGA is big. The compiler needs to configure everything in its whole chip, i.e., in our case, it mostly deactivates non-used parts.

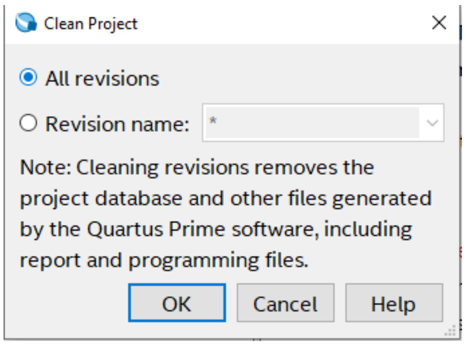
We can reduce the project size by removing temporary files before zipping or copying the project to a USB stick by the Project -> Clean Project, equivalent to the "make clean" command in classic programming.



Any of the selections below leads to removing all Quartus compiler temporary files.



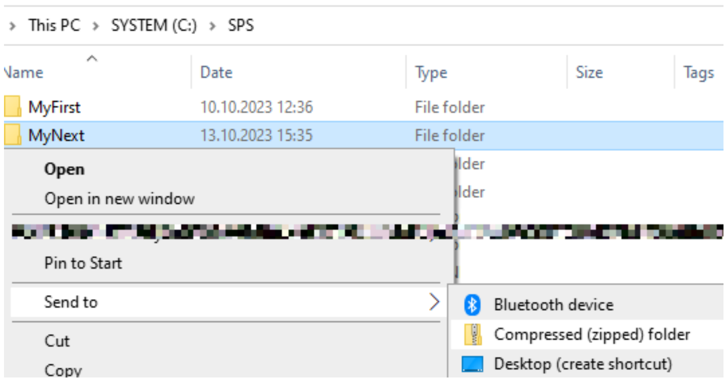
Note: Cleaning revisions removes the project database and other files generated by the Quartus Prime software, including report and programming files.



Note: Cleaning revisions removes the project database and other files generated by the Quartus Prime software, including report and programming files.

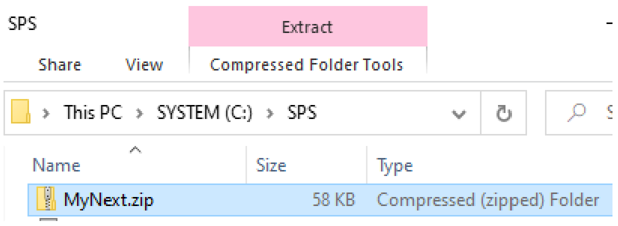
Then, we close the Quartus to release its locked files and run the File Explorer.

We select the Send to->Compressed (zipped) folder from the context menu of the root directory folder.


This PC > SYSTEM (C:) > SPS
Open
Open in new window
[redacted]
Pin to Start
Send to
Cut
Copy
Bluetooth device
Compressed (zipped) folder
Desktop (create shortcut)

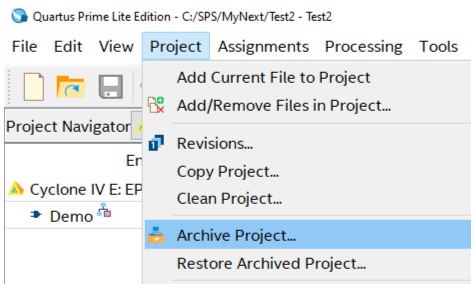
Name	Date	Type	Size	Tags
MyFirst	10.10.2023 12:36	File folder		
MyNext	13.10.2023 15:35	File folder		

The result of the compression:



Name	Size	Type
MyNext.zip	58 KB	Compressed (zipped) Folder

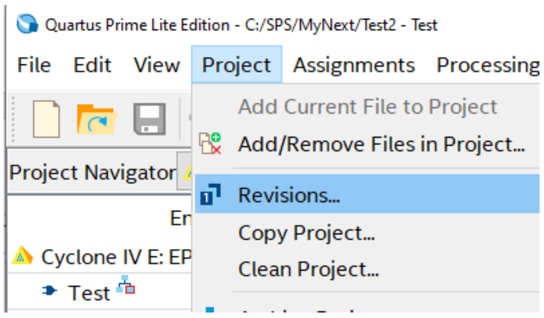
Note: We prefer zip to the Quartus menu command the "Archive Project":

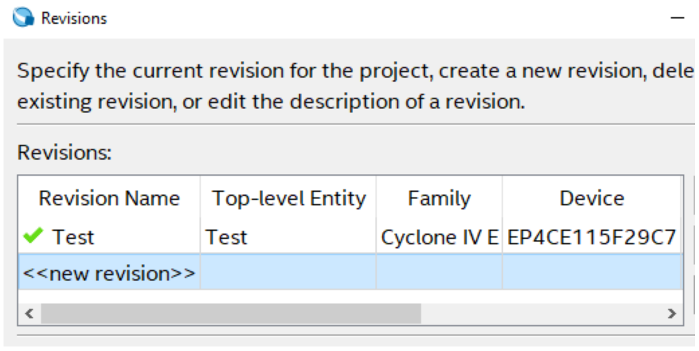


*Its result has an internal format *.qar that can be depacked only by Quartus. The zip file is more versatile.*

6.4 Changing Revision = Compilation Result Filename

The compilation generates the result, which filename is derived from the revision name. For example, the result can be Test.sof (sof=SRAM Object File). The Revision is also copied with the project. We can quickly change it from the Revision dialog:


Quartus Prime Lite Edition - C:/SPS/MyNext/Test2 - Test
File Edit View Project Assignments Processing
Add Current File to Project
Add/Remove Files in Project...
Revisions...
Copy Project...
Clean Project...
Project Navigator
Cyclone IV E: EP
Test

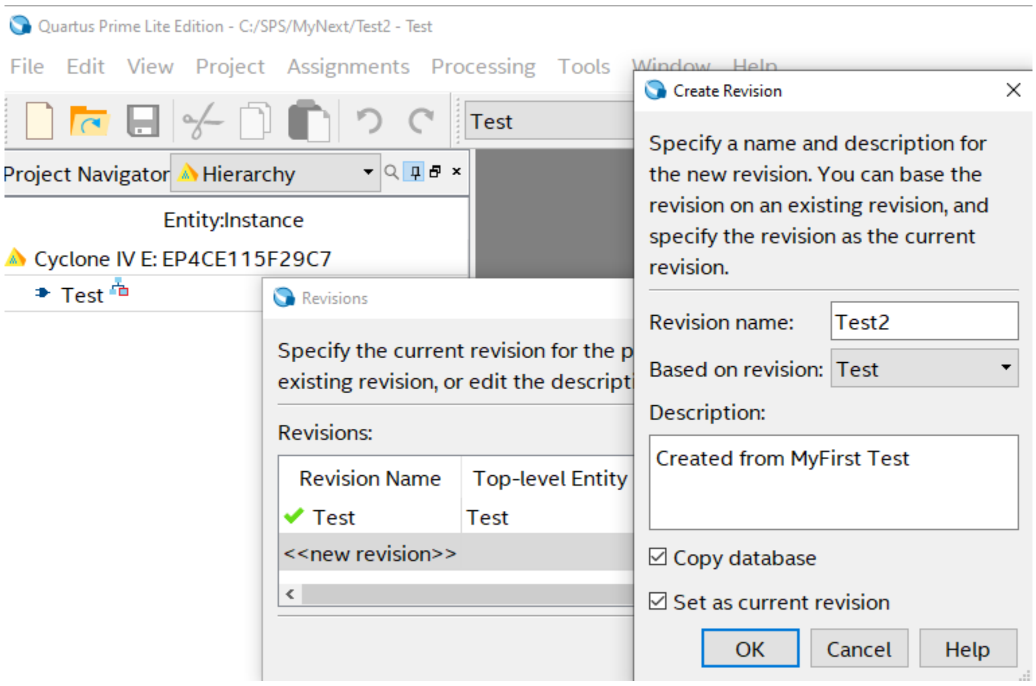


Specify the current revision for the project, create a new revision, dele
existing revision, or edit the description of a revision.

Revisions:

Revision Name	Top-level Entity	Family	Device
✓ Test	Test	Cyclone IV E	EP4CE115F29C7
<<new revision>>			

By mouse double click into <<new revision>> table row, we open sub dialog:


Quartus Prime Lite Edition - C:/SPS/MyNext/Test2 - Test
File Edit View Project Assignments Processing Tools Window Help
Test
Project Navigator
Hierarchy
Entity:Instance
Cyclone IV E: EP4CE115F29C7
Test
Revisions
Create Revision
OK
Cancel
Help

Specify the current revision for the p
existing revision, or edit the descript

Revisions:

Revision Name	Top-level Entity
✓ Test	Test
<<new revision>>	

Specify a name and description for the new revision. You can base the revision on an existing revision, and specify the revision as the current revision.

Revision name: Test2

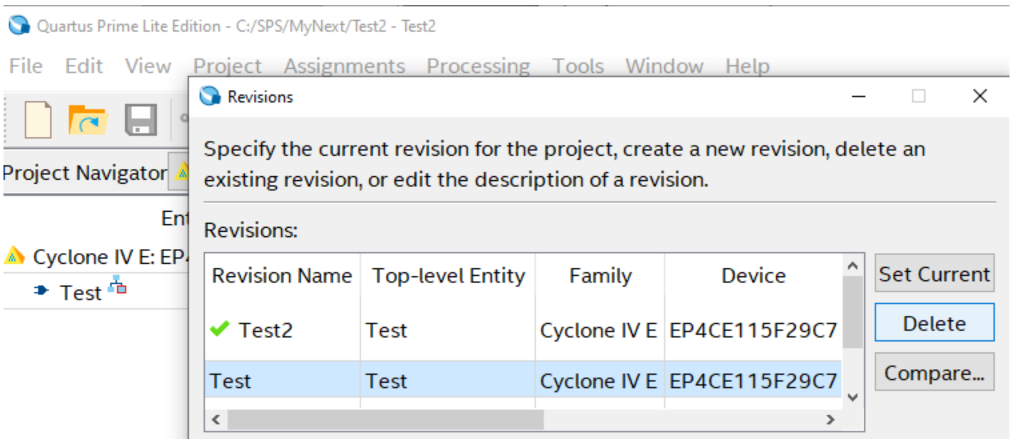
Based on revision: Test

Description: Created from MyFirst Test

☑ Copy database

☑ Set as current revision

We enter, for example, Test2 as the name of our new project and possibly some description if we wish. After confirming by [OK], we again open the menu: Project ->Revisions.

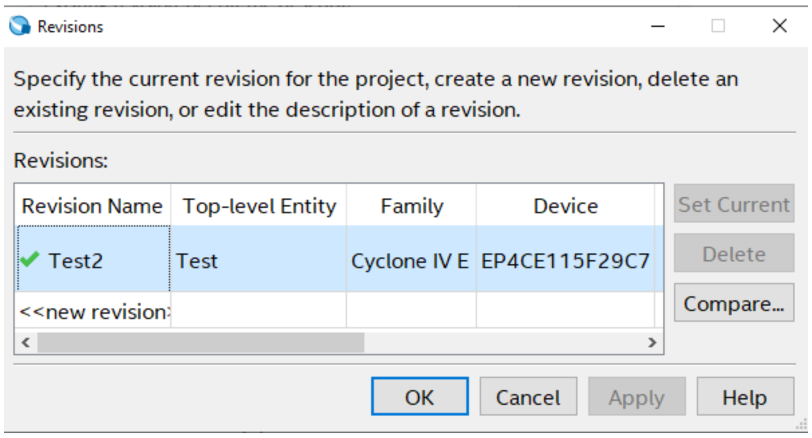

Quartus Prime Lite Edition - C:/SPS/MyNext/Test2 - Test2
File Edit View Project Assignments Processing Tools Window Help
Project Navigator
Cyclone IV E: EP
Test
Revisions
Set Current
Delete
Compare...

Specify the current revision for the project, create a new revision, delete an
existing revision, or edit the description of a revision.

Revisions:

Revision Name	Top-level Entity	Family	Device
✓ Test2	Test	Cyclone IV E	EP4CE115F29C7
Test	Test	Cyclone IV E	EP4CE115F29C7

After deleting the old revision Test, we obtained the project, which compilation leads to Test2.sof.

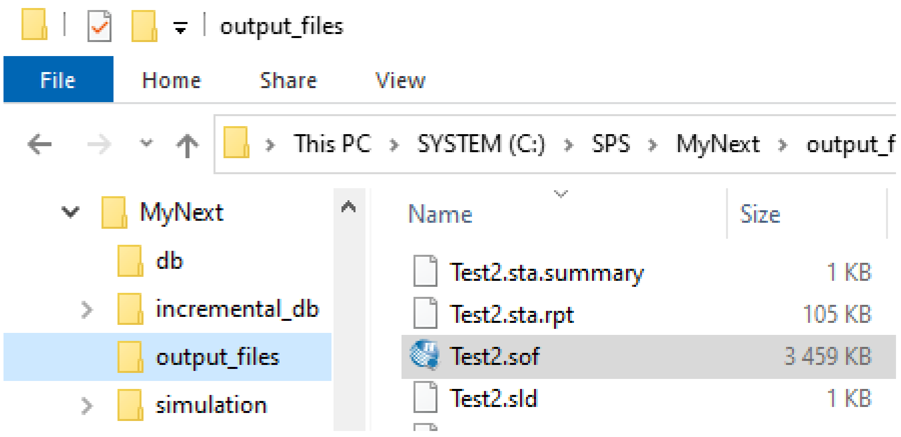

Revisions

Specify the current revision for the project, create a new revision, delete an existing revision, or edit the description of a revision.

Revisions:

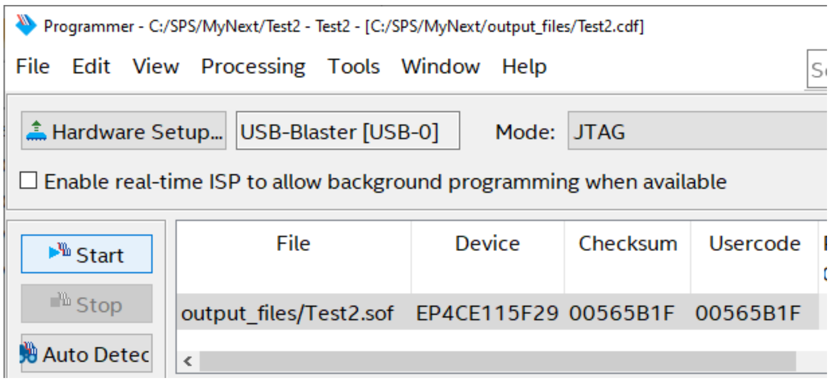
Revision Name	Top-level Entity	Family	Device
✓ Test2	Test	Cyclone IV E	EP4CE115F29C7
<<new revision			

The result Test2.sof can be downloaded into the FPGA chip by the Quartus programmer.



Name	Size
Test2.sta.summary	1 KB
Test2.sta.rpt	105 KB
Test2.sof	3 459 KB
Test2.sld	1 KB

The Quartus menu: Tools->Programmer shows the dialog below.


Programmer - C:/SPS/MyNext/Test2 - Test2 - [C:/SPS/MyNext/output_files/Test2.cdf]

USB-Blaster [USB-0] Mode: JTAG

☐ Enable real-time ISP to allow background programming when available

File	Device	Checksum	Usercode
output_files/Test2.sof	EP4CE115F29	00565B1F	00565B1F

We explain its setting in practical exercises of our LSP course. Its brief explanation is on page 40 of the document:

https://dcenet.fel.cvut.cz/edu/fpga/de2-115/My_First_Fpga.pdf

Note: VEEK-MT2 is a combo of LCD and DE2-115 board; thus, DE2-115 manuals are valid, but DE2-115 Pin Assignments define only a part of VEEK-MT2 pin assignments.

The programmer's more advanced functions, which we do not use in the LSP course, are described in the Intel document:

https://www.intel.com/content/www/us/en/docs/programmable/683039/20-4/introduction.html

~ o ~

*** The End ***